

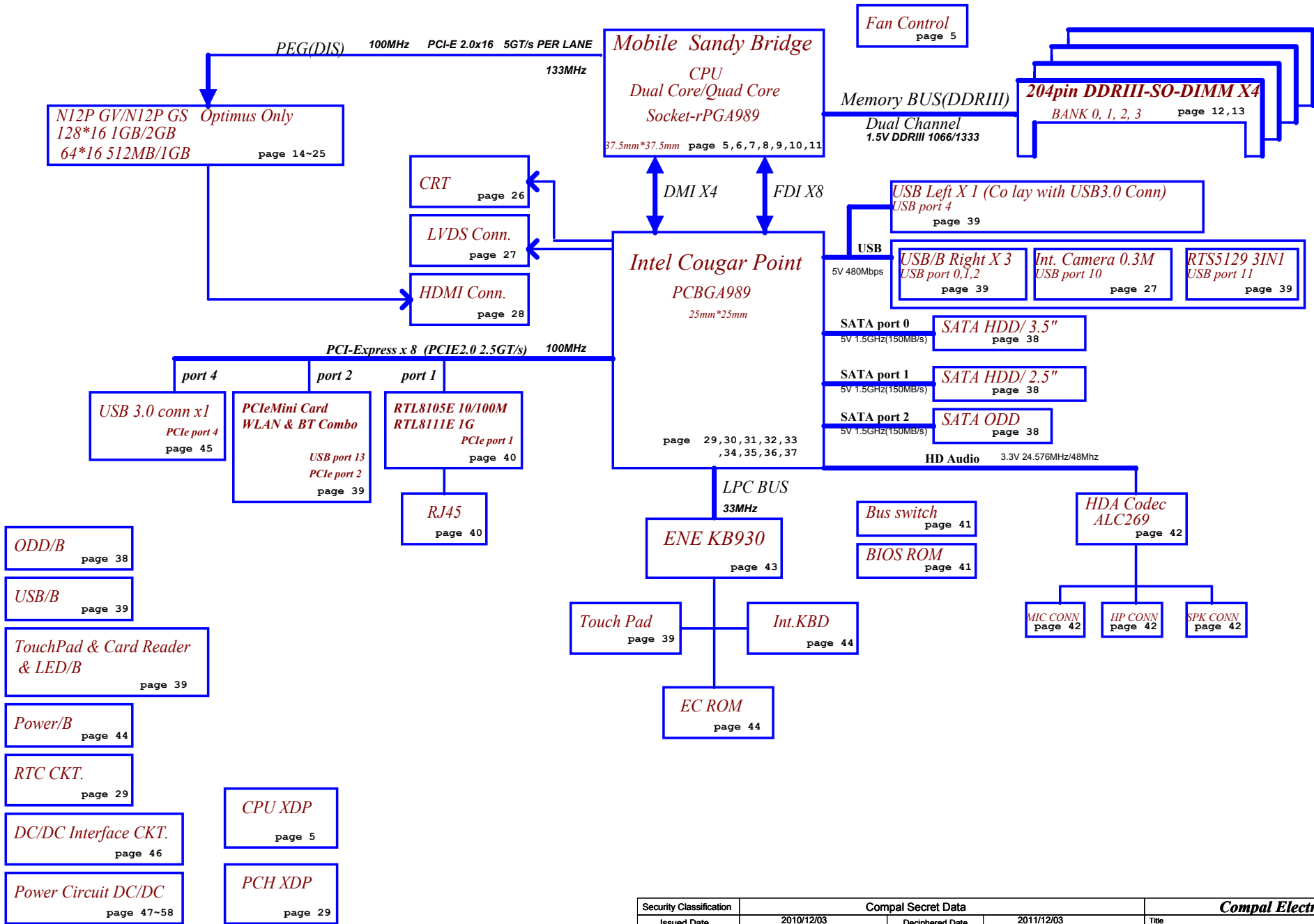
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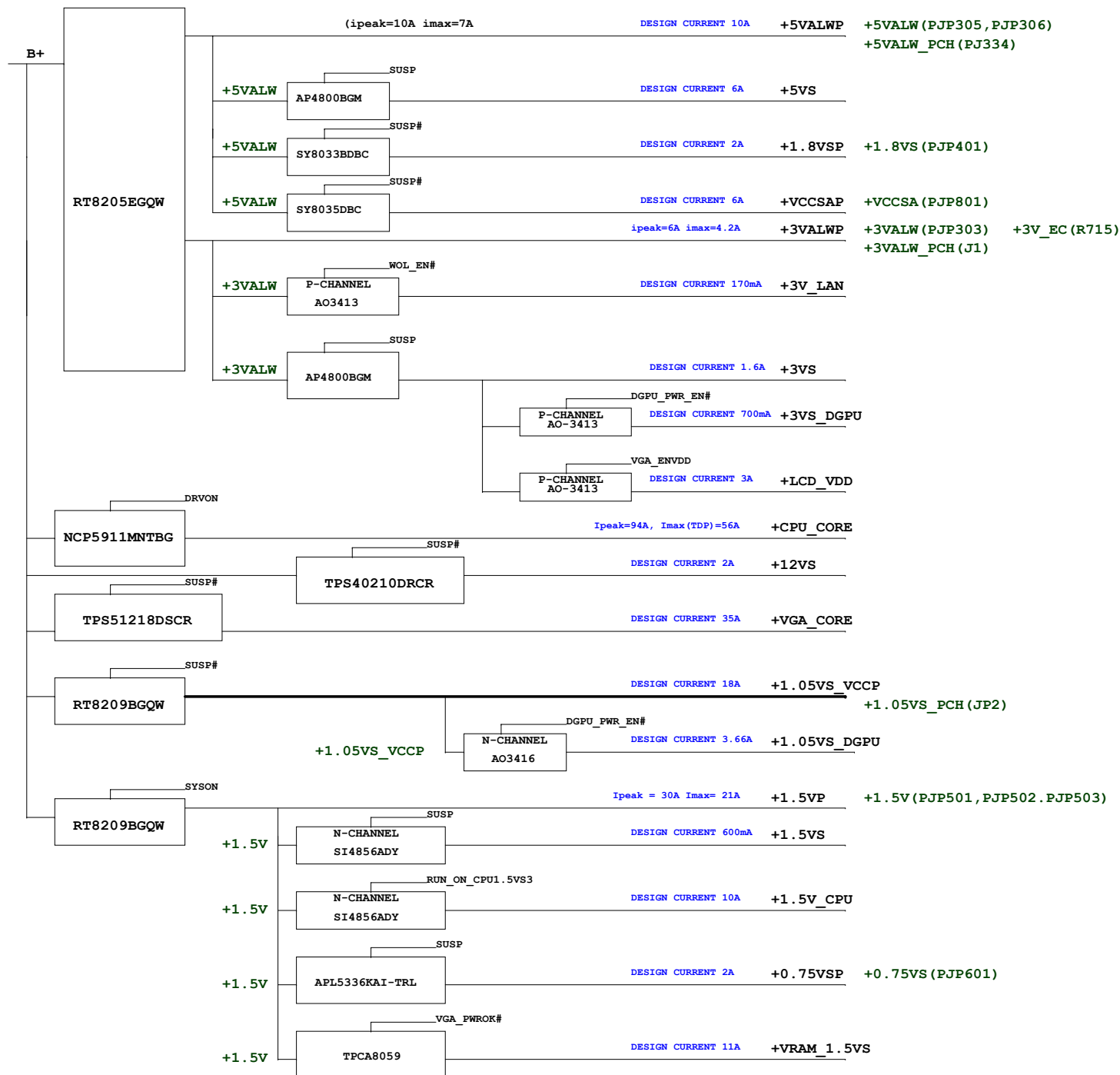
PBL80 Project

LA-7441P REV 0.1 Schematic

Intel Sandy Bridge/Cougar Point
N12P-GV/GS-Optimus Only
2011-01-21 Rev. 0.1

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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +5VALW_PCH +3VALW_PCH +3V_LAN +3V_EC +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS_VCCP +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VCCSA +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +12VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMMA1	A0 H	1010 0000 b
+3VS	DDR SO-DIMMA2	A0 H	1010 0010 b
+3VS	DDR SO-DIMMB1	A4 H	1010 0100 b
+3VS	DDR SO-DIMMB2	A0 H	1010 0110 b
+3VS	WLAN		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
				+3VS	VGA Thermal Sensor	9A H	1001 1010 b

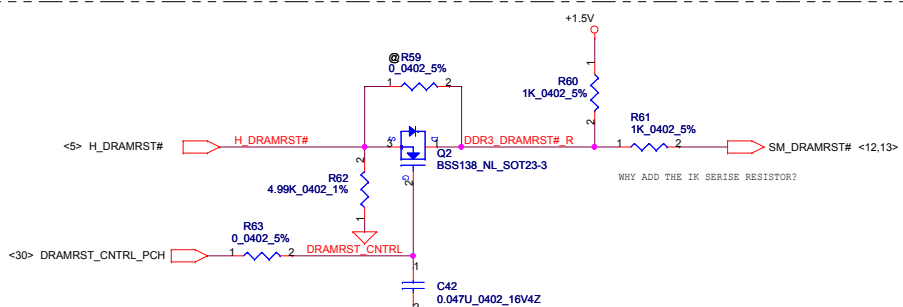
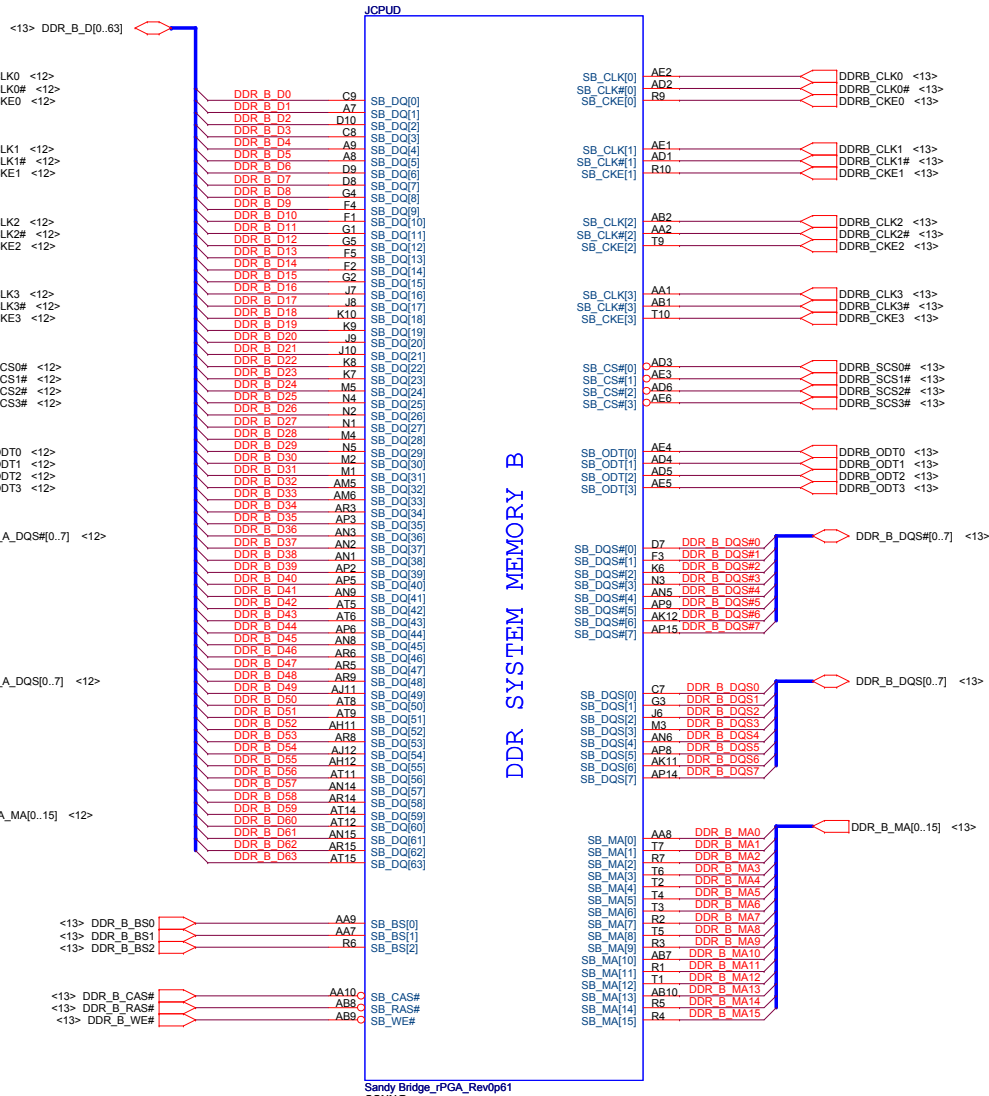
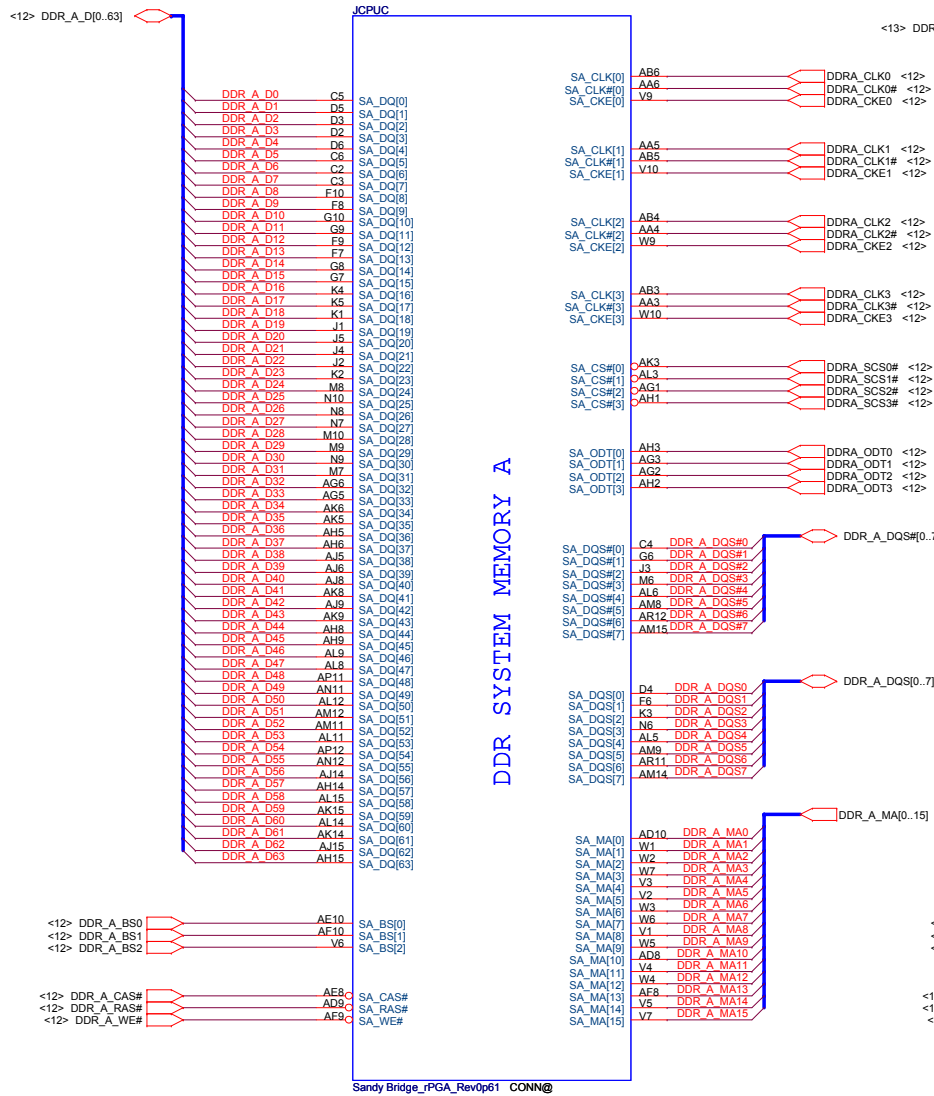
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

Function	VRAM					GPU		Board ID
description	VRAM	Samsung 64bits	Hynix 64bits	Samsung 128bits	Hynix 128bits	N12P-GS	N12P-GV	Adaptor
explain	VRAM	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Adaptor
BTO	8PCS@	PD 20K	PD 15K	PD 45.3K	PD 34.8K	N12PGS@	N12PGV@	90W@, 120W@

Function	Crisis recovery	HDMI	WLAN+BT		LAN	
description	BUS SWITCH	HDMI	WLAN+BT (BT pin 51)	WLAN+BT (BT pin 5)	Giga LAN	10/100M LAN
explain	BUS SWITCH	HDMI	WLAN+BT (BT pin 51)	WLAN+BT (BT pin 5)	Strap pin	Strap pin
BTO	Debug@	HDMI@	BT@	COMBO@	8111E@	8105E@

Function	USB3.0/2.0 Colay		SATA3.0 Repeater Chip		SATA Preemphasis		SATA Equalization	
description	USB3.0	USB2.0	MAXIM	TI	Preemphasis		Equalization	
explain	USB3.0	USB2.0	MAX4951	SN75LVCP601	Enable	Disable	Maximum	Normal
BTO	USB3@	USB2@	MAXIM@	TI@	DEN@	NDEN@	EQ@	NEQ@

Function	SATA path	
description	PCH	Repeater
explain	PCH	Repeater
BTO	SATA@	SATARP@



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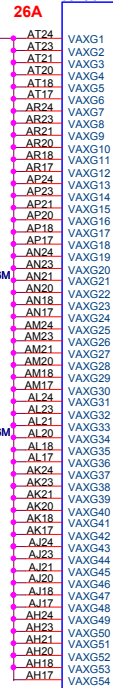
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Sandy Bridge(3/6)-DDR III

PBL80 LA-7441P M/B

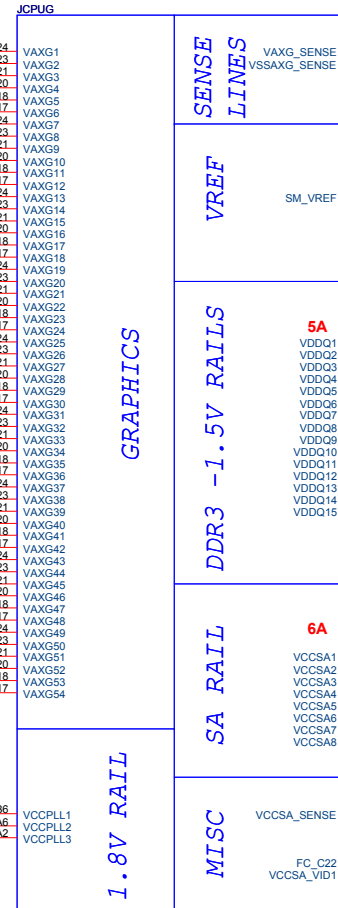
Rev 0.1


```
2 x 330  $\mu$ F on Bottom socket edge
Bottom Socket Cavity 22U 0805 *2
Bottom Socket Edge 22U 0805 *4
Top Socket Cavity 22U 0805 *2
Top Socket Edge 22U 0805 *4
```

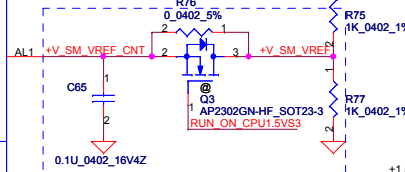


```
1 x 330 µF
Bottom Socket Edge
1U 0402 *1
10U 0805 *1
```

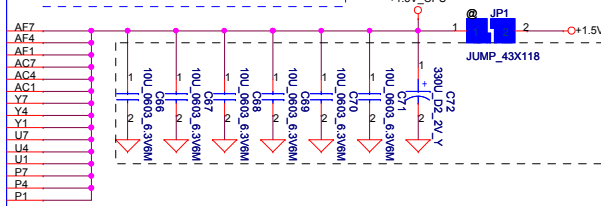
GRAPHICS



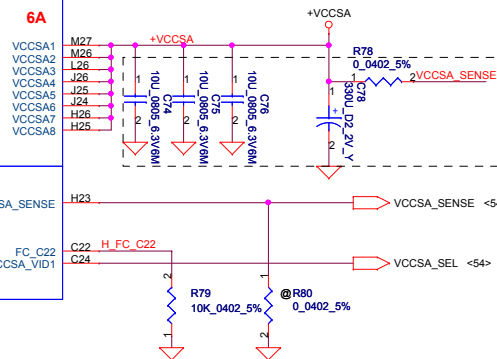
Sandy Bridge_rPGA_Rev0p61
CONN@



```
| +V_SM_VREF should have 20  
| mil trace width
```



Material Note (VDDQ)
Bottom Socket Edge
1 x 330 μ F
10U 0805 *6



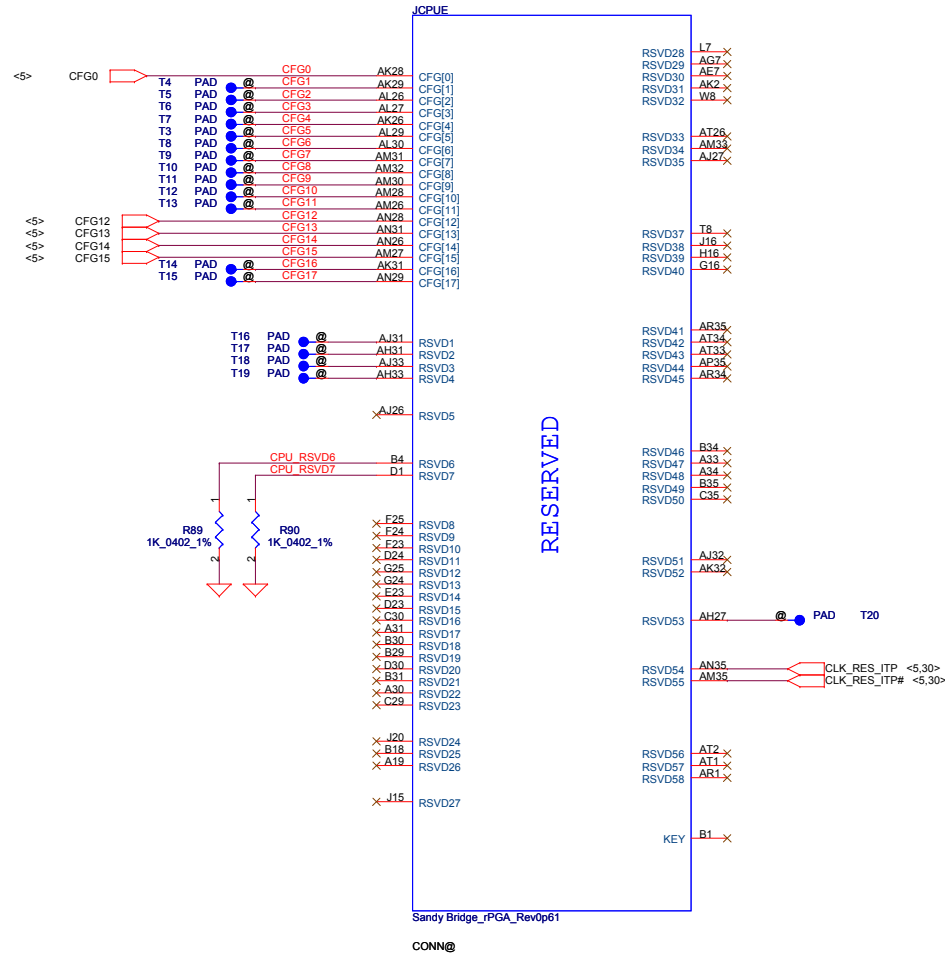
1 x 330 μ F
Bottom Socket Cavity 10U 0805 *2
Bottom Socket Edge 10U 0805 *1

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Sandy Bridge(4/6)-PWR

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CFG Straps for Processor

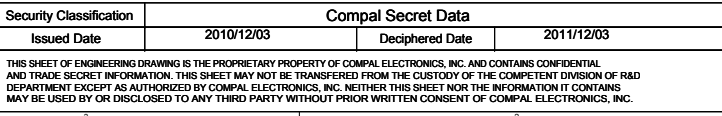


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

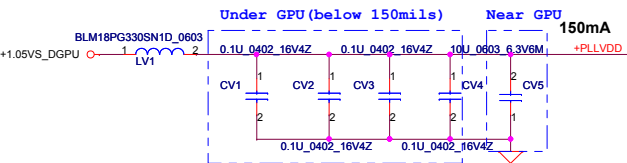
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



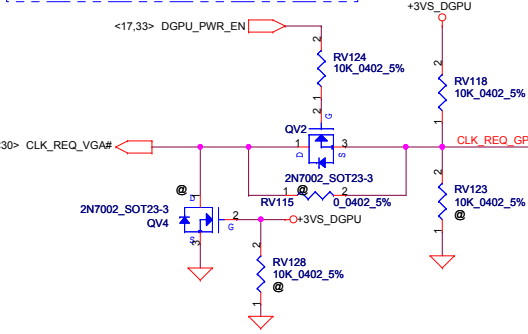
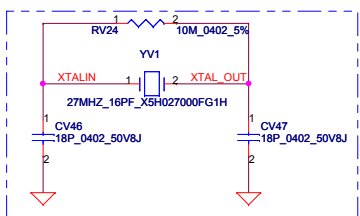
N12PGS@
UV1
N12P-GS-A1_BGA_973P



PCIE GTX_C_CRX_P0	CV6	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P0	AL17
PCIE GTX_C_CRX_N0	CV7	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N0	AM17
PCIE GTX_C_CRX_P1	CV8	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P1	AM18
PCIE GTX_C_CRX_N1	CV9	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N1	AM19
PCIE GTX_C_CRX_P2	CV10	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P2	AL19
PCIE GTX_C_CRX_N2	CV11	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N2	AK19
PCIE GTX_C_CRX_P3	CV12	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P3	AL20
PCIE GTX_C_CRX_N3	CV13	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N3	AM20
PCIE GTX_C_CRX_P4	CV14	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P4	AM21
PCIE GTX_C_CRX_N4	CV15	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N4	AM22
PCIE GTX_C_CRX_P5	CV16	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P5	AM23
PCIE GTX_C_CRX_N5	CV17	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N5	AK22
PCIE GTX_C_CRX_P6	CV18	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P6	AL23
PCIE GTX_C_CRX_N6	CV19	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N6	AM23
PCIE GTX_C_CRX_P7	CV20	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P7	AM24
PCIE GTX_C_CRX_N7	CV21	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N7	AM25
PCIE GTX_C_CRX_P8	CV22	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P8	AL25
PCIE GTX_C_CRX_N8	CV23	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N8	AK25
PCIE GTX_C_CRX_P9	CV24	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P9	AL26
PCIE GTX_C_CRX_N9	CV25	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N9	AM26
PCIE GTX_C_CRX_P10	CV26	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P10	AM27
PCIE GTX_C_CRX_N10	CV27	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N10	AM28
PCIE GTX_C_CRX_P11	CV28	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P11	AL28
PCIE GTX_C_CRX_N11	CV29	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N11	AK28
PCIE GTX_C_CRX_P12	CV30	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P12	AL29
PCIE GTX_C_CRX_N12	CV31	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N12	AM29
PCIE GTX_C_CRX_P13	CV32	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P13	AM29
PCIE GTX_C_CRX_N13	CV33	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N13	AM30
PCIE GTX_C_CRX_P14	CV34	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P14	AM31
PCIE GTX_C_CRX_N14	CV35	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N14	AM32
PCIE GTX_C_CRX_P15	CV36	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_P15	AN32
PCIE GTX_C_CRX_N15	CV37	1	2	0.22U_0402_10V8K	PCIE GTX_C_CRX_N15	AP32

<30> CLK_PCIE_VGA#
<30> CLK_PCIE_GPU#

RV19 stuff per NV request.
12/17



Internal Thermal Sensor
<15> SMB_CLK_GPU
<15> SMB_DATA_GPU
VGA_EDID_CLK_F3
VGA_EDID_DATA_F4
I2CB_SCL_G3
I2CB_SDA_G2
I2CA_SCL_G1
I2CA_SDA_G4
HDCP_SCL_F6
HDCP_SDA_G6

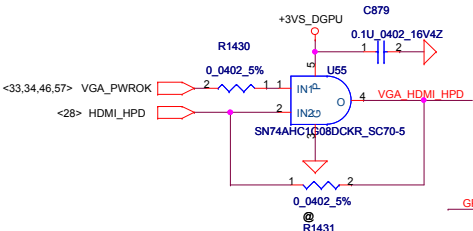
PCIE CTX_C_CRX_P0	AP17
PCIE CTX_C_CRX_N0	AN17
PCIE CTX_C_CRX_P1	AP18
PCIE CTX_C_CRX_N1	AN18
PCIE CTX_C_CRX_P2	AP19
PCIE CTX_C_CRX_N2	AN19
PCIE CTX_C_CRX_P3	AP20
PCIE CTX_C_CRX_N3	AN20
PCIE CTX_C_CRX_P4	AP21
PCIE CTX_C_CRX_N4	AN21
PCIE CTX_C_CRX_P5	AP22
PCIE CTX_C_CRX_N5	AN22
PCIE CTX_C_CRX_P6	AP23
PCIE CTX_C_CRX_N6	AN23
PCIE CTX_C_CRX_P7	AP24
PCIE CTX_C_CRX_N7	AN24
PCIE CTX_C_CRX_P8	AP25
PCIE CTX_C_CRX_N8	AN25
PCIE CTX_C_CRX_P9	AP26
PCIE CTX_C_CRX_N9	AN26
PCIE CTX_C_CRX_P10	AP27
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PCIE CTX_C_CRX_P11	AP28
PCIE CTX_C_CRX_N11	AN28
PCIE CTX_C_CRX_P12	AP29
PCIE CTX_C_CRX_N12	AN29
PCIE CTX_C_CRX_P13	AP30
PCIE CTX_C_CRX_N13	AN30
PCIE CTX_C_CRX_P14	AP31
PCIE CTX_C_CRX_N14	AN31
PCIE CTX_C_CRX_P15	AP32
PCIE CTX_C_CRX_N15	AN32

Part 1 of 7
GPIO
PCI EXPRESS
DVO

CLK
I2C
DACs

GPIO0	K1	VGA_GPIO1
GPIO1	K2	
GPIO2	K3	
GPIO3	K4	
GPIO4	K5	GPU_VID0
GPIO5	K6	GPU_VID1
GPIO6	K7	
GPIO7	K8	GPIO8
GPIO8	K9	THERM#_VGA
GPIO9	K10	
GPIO10	K11	
GPIO11	K12	
GPIO12	K13	TV1
GPIO13	K14	VGA_HDMI_HPD
GPIO14	K15	
GPIO15	K16	
GPIO16	K17	
GPIO17	K18	
GPIO18	K19	
GPIO19	K20	
GPIO20	K21	
GPIO21	K22	
GPIO22	K23	
GPIO23	K24	
GPIO24	K25	
MIOA_D0_NC	N1	
MIOA_D1_NC	N2	
MIOA_D2_NC	N3	
MIOA_D3_NC	N4	
MIOA_D4_NC	N5	
MIOA_D5_NC	N6	
MIOA_D6_NC	N7	
MIOA_D7_NC	N8	
MIOA_D8_NC	N9	
MIOA_D9_NC	N10	
MIOA_D10_NC	N11	
MIOA_D11_NC	N12	
MIOA_D12_NC	N13	
MIOA_D13_NC	N14	
MIOA_D14_NC	N15	
MIOB_D0_NC	Y1	
MIOB_D1_NC	Y2	
MIOB_D2_NC	Y3	
MIOB_D3_NC	Y4	
MIOB_D4_NC	Y5	
MIOB_D5_NC	Y6	
MIOB_D6_NC	Y7	
MIOB_D7_NC	Y8	
MIOB_D8_NC	Y9	
MIOB_D9_NC	Y10	
MIOB_D10_NC	Y11	
MIOB_D11_NC	Y12	
MIOB_D12_NC	Y13	
MIOB_D13_NC	Y14	
MIOB_D14_NC	Y15	
MIOA_HSNC_NC	N16	
MIOA_VSNC_NC	N17	
MIOB_HSNC_NC	Y16	
MIOB_VSNC_NC	Y17	
MIOA_DE_NC	N18	
MIOA_CTL3_NC	N19	
MIOA_VREF_NC	N20	
MIOB_DE_NC	Y18	
MIOB_CTL3_NC	Y19	
MIOB_VREF_NC	Y20	
MIOA_CLKIN_NC	N21	
MIOA_CLKOUT_NC	N22	
MIOB_CLKIN_NC	Y21	
MIOB_CLKOUT_NC	Y22	
MIOA_CLKOUT_NC_NC	N23	
MIOB_CLKOUT_NC_NC	N24	
MIOACAL_PD_VDDQ_NC	N25	
MIOACAL_PD_GND_NC	N26	
MIOBCAL_PD_VDDQ_NC	N27	
MIOBCAL_PD_GND_NC	N28	
DACA_RED	AM15	
DACA_GREEN	AM14	
DACA_BLUE	AL14	
DACA_HSNC	AM13	
DACA_VSYNC	AL13	
DACA_VDD	AK12	
DACA_VREF	AK13	
DACB_RED	AK4	
DACB_GREEN	AL4	
DACB_BLUE	AL4	
DACB_HSNC	AM1	
DACB_VSYNC	AM2	
DACB_VDD	AG7	
DACB_VREF	AK5	
DACB_RSET	AH7	

<6> PCIE GTX_C_CRX_P[0..15]
<6> PCIE GTX_C_CRX_N[0..15]
<6> PCIE CTX_C_CRX_P[0..15]
<6> PCIE CTX_C_CRX_N[0..15]

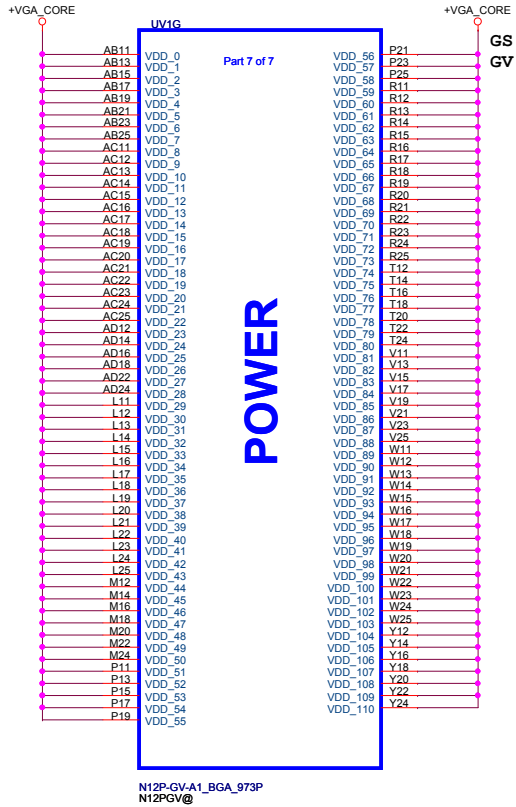


GPIO8
GPIO12
VGA_EDID_CLK
VGA_EDID_DATA
SMB_CLK_GPU
SMB_DATA_GPU
THERM#_VGA
HDCP_SCL
HDCP_SDA
I2CA_SDA
I2CA_SCL
I2CB_SCL
I2CB_SDA
VGA_GPIO1
VGA_HDMI_HPD

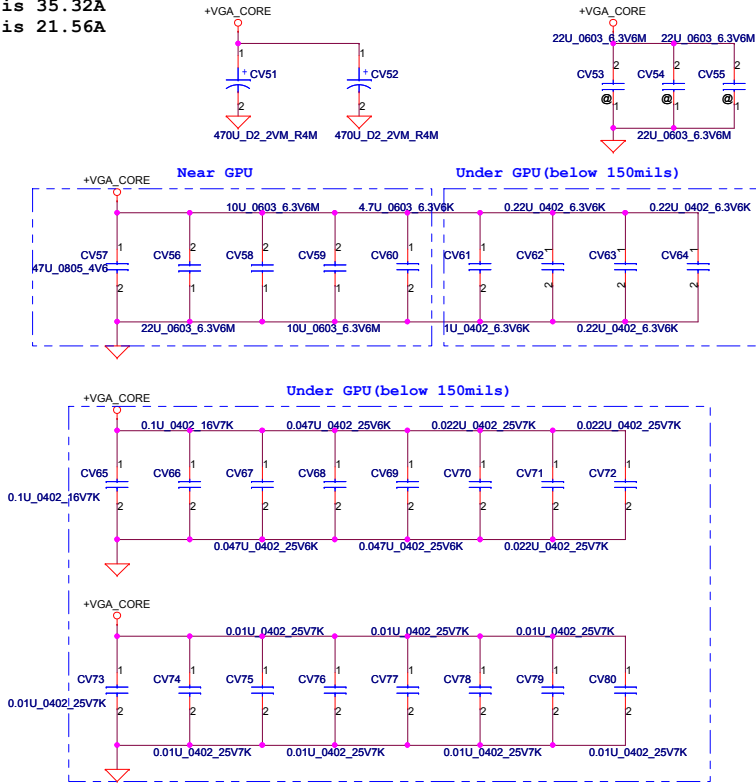
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VGA(1/12)-PCIE/DAC/GPIO	
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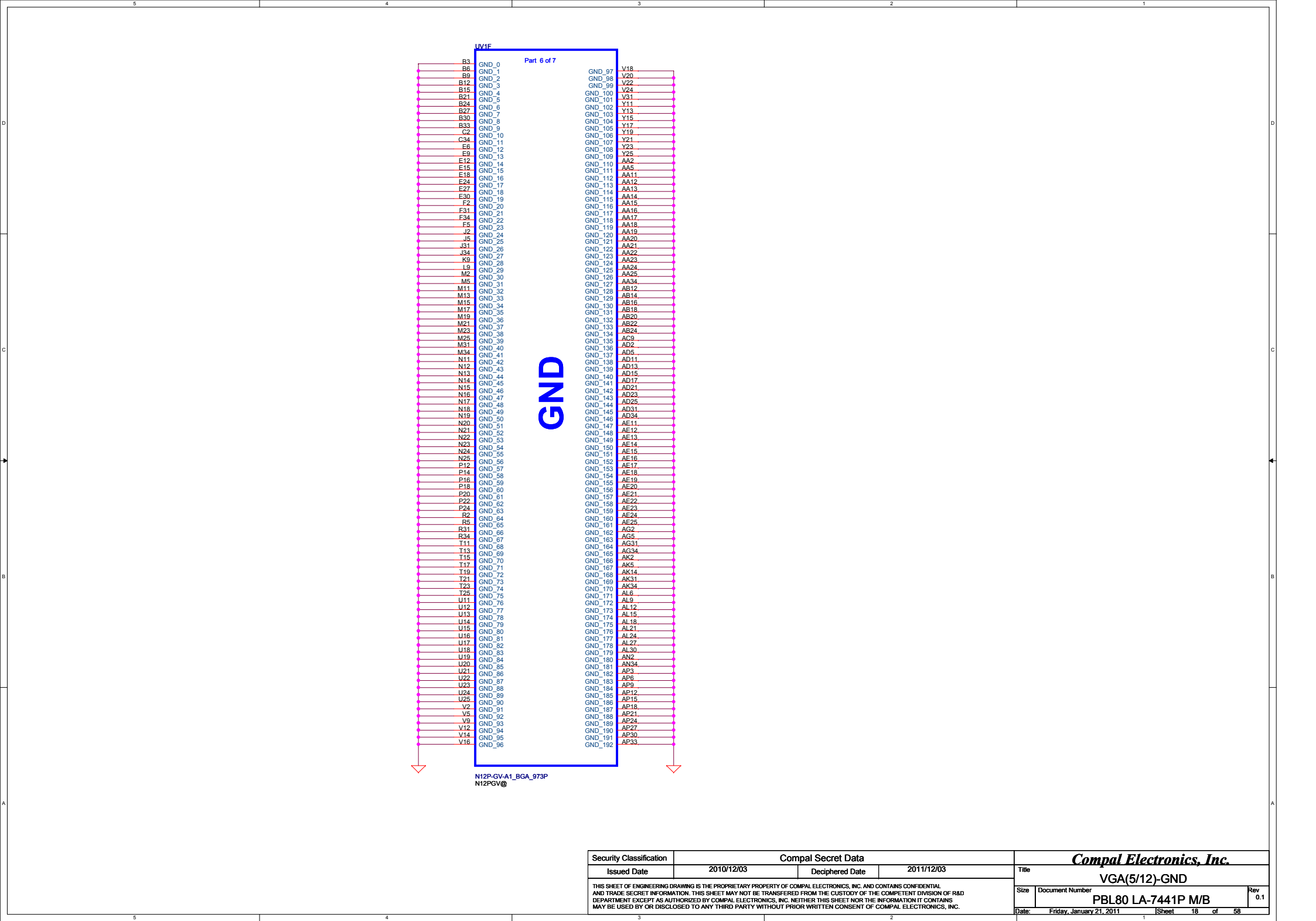
Pstate	GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
P8-P12	0	0	0.825V	0.85V
P0 (Hot)	1	0	0.975V	1V
	0	1		
P0 (cold)	1	1	1V	1.025V



GS EDP Peak is 35.32A
GV EDP Peak is 21.56A



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				Deciphered Date				VGA(3/12)-VGA CORE			
				2011/12/03				Size			
								Document Number			
								PBL80 LA-7441P M/B			
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								Rev			
								0.1			



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Issued Date		2010/12/03		Deciphered Date		2011/12/03		Title			
								VGA(5/12)-GND			
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								PBL80 LA-7441P M/B		0.1	
						Date:		Friday, January 21, 2011		Sheet 18 of 58	

<21,22> MDA[0..63] ← MDA[0..63]

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MDA1 N33 FBA_D1
MDA2 L33 FBA_D2
MDA3 N34 FBA_D3
MDA4 N35 FBA_D4
MDA5 P36 FBA_D5
MDA6 P33 FBA_D6
MDA7 P34 FBA_D7
MDA8 K35 FBA_D8
MDA9 K33 FBA_D9
MDA10 K34 FBA_D10
MDA11 H33 FBA_D11
MDA12 G34 FBA_D12
MDA13 G33 FBA_D13
MDA14 E34 FBA_D14
MDA15 E33 FBA_D15
MDA16 G31 FBA_D16
MDA17 F30 FBA_D17
MDA18 G30 FBA_D18
MDA19 G32 FBA_D19
MDA20 K30 FBA_D20
MDA21 K32 FBA_D21
MDA22 H30 FBA_D22
MDA23 K31 FBA_D23
MDA24 L31 FBA_D24
MDA25 L30 FBA_D25
MDA26 M32 FBA_D26
MDA27 N30 FBA_D27
MDA28 M30 FBA_D28
MDA29 P31 FBA_D29
MDA30 R32 FBA_D30
MDA31 R30 FBA_D31
MDA32 G30 FBA_D32
MDA33 AG32 FBA_D33
MDA34 AH31 FBA_D34
MDA35 AF31 FBA_D35
MDA36 AE30 FBA_D36
MDA37 AE30 FBA_D37
MDA38 AC32 FBA_D38
MDA39 AD30 FBA_D39
MDA40 AN33 FBA_D40
MDA41 AL31 FBA_D41
MDA42 AM33 FBA_D42
MDA43 AL33 FBA_D43
MDA44 AK30 FBA_D44
MDA45 AK32 FBA_D45
MDA46 AJ30 FBA_D46
MDA47 AH30 FBA_D47
MDA48 AH33 FBA_D48
MDA49 AH35 FBA_D49
MDA50 AH34 FBA_D50
MDA51 AH32 FBA_D51
MDA52 AJ33 FBA_D52
MDA53 AL35 FBA_D53
MDA54 AM34 FBA_D54
MDA55 AM35 FBA_D55
MDA56 AF33 FBA_D56
MDA57 AE32 FBA_D57
MDA58 AE34 FBA_D58
MDA59 AE35 FBA_D59
MDA60 AE34 FBA_D60
MDA61 AE33 FBA_D61
MDA62 AB32 FBA_D62
MDA63 AC35 FBA_D63

Part 2 of 7

MEMORY INTERFACE

UV1B

FBA_CMD0 U30 CMDA0
FBA_CMD1 V30 CMDA2
FBA_CMD2 U31 CMDA3
FBA_CMD3 V32 CMDA4
FBA_CMD4 T35 CMDA5
FBA_CMD5 U33 CMDA6
FBA_CMD6 W32 CMDA7
FBA_CMD7 W33 CMDA8
FBA_CMD8 W31 CMDA9
FBA_CMD9 W34 CMDA10
FBA_CMD10 U34 CMDA11
FBA_CMD11 U35 CMDA12
FBA_CMD12 U32 CMDA13
FBA_CMD13 T33 CMDA14
FBA_CMD14 FBA_CMD14 T33 CMDA15
FBA_CMD15 W30 CMDA16
FBA_CMD16 AB30
FBA_CMD17 AA30
FBA_CMD18 AB31
FBA_CMD19 AA32
FBA_CMD20 AB33
FBA_CMD21 Y32
FBA_CMD22 Y33
FBA_CMD23 AB34
FBA_CMD24 AB35
FBA_CMD25 Y35
FBA_CMD26 Y34
FBA_CMD27 Y31
FBA_CMD28 Y30
FBA_CMD29 W29
FBA_CMD30 Y29
FBA_CMD31 Y29
FBA_DQM0 P32
FBA_DQM1 H34
FBA_DQM2 J30
FBA_DQM3 P30
FBA_DQM4 AF32
FBA_DQM5 AL32
FBA_DQM6 AL34
FBA_DQM7 AF35
FBA_DQS_RN0 L35
FBA_DQS_RN1 G35
FBA_DQS_RN2 H31
FBA_DQS_RN3 N32
FBA_DQS_RN4 AD32
FBA_DQS_RN5 AJ31
FBA_DQS_RN6 AJ35
FBA_DQS_RN7 AC34
FBA_DQS_WP0 L34
FBA_DQS_WP1 H35
FBA_DQS_WP2 J32
FBA_DQS_WP3 N31
FBA_DQS_WP4 AE31
FBA_DQS_WP5 AJ32
FBA_DQS_WP6 AJ34
FBA_DQS_WP7 AC33
FBA_WCK0 P29
FBA_WCK0_N R29
FBA_WCK1 L29
FBA_WCK1_N M29
FBA_WCK2 AG29
FBA_WCK2_N AH29
FBA_WCK3 AD29
FBA_WCK3_N AE29
FBA_CLK0 T32
FBA_CLK0_N T31
FBA_CLK1 AC31
FBA_CLK1_N AC30

CMDA0 <21>
CMDA2 <21>
CMDA3 <21>
CMDA4 <21,22>
CMDA5 <21,22>
CMDA6 <21,22>
CMDA7 <21,22>
CMDA8 <21,22>
CMDA9 <21,22>
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CMDA24 <21,22>
CMDA25 <21,22>
CMDA26 <21,22>
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CMDA28 <21,22>
CMDA29 <21,22>
CMDA30 <21,22>

DQMA[7..0] <21,22>

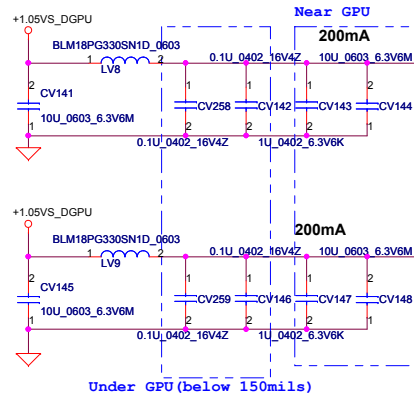
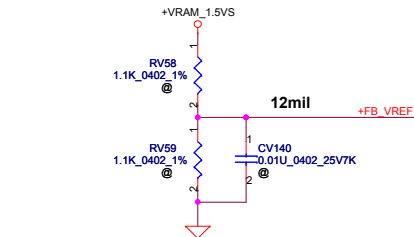
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DQSA[7..0] <21,22>

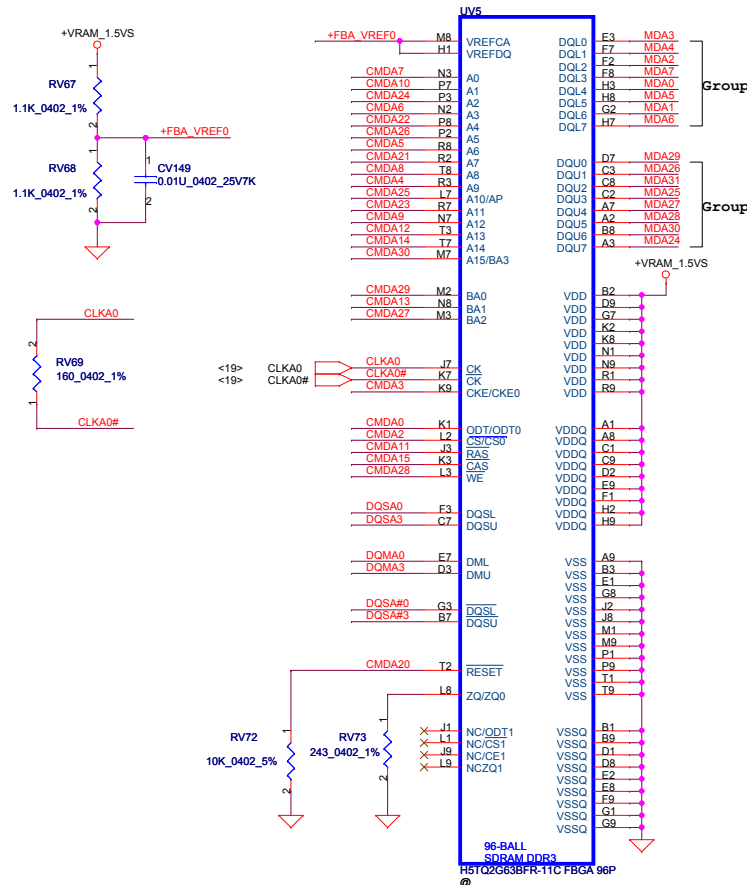
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CLKA0# <21>
CLKA1 <22>
CLKA1# <22>

Mode E - Mirror Mode Mapping

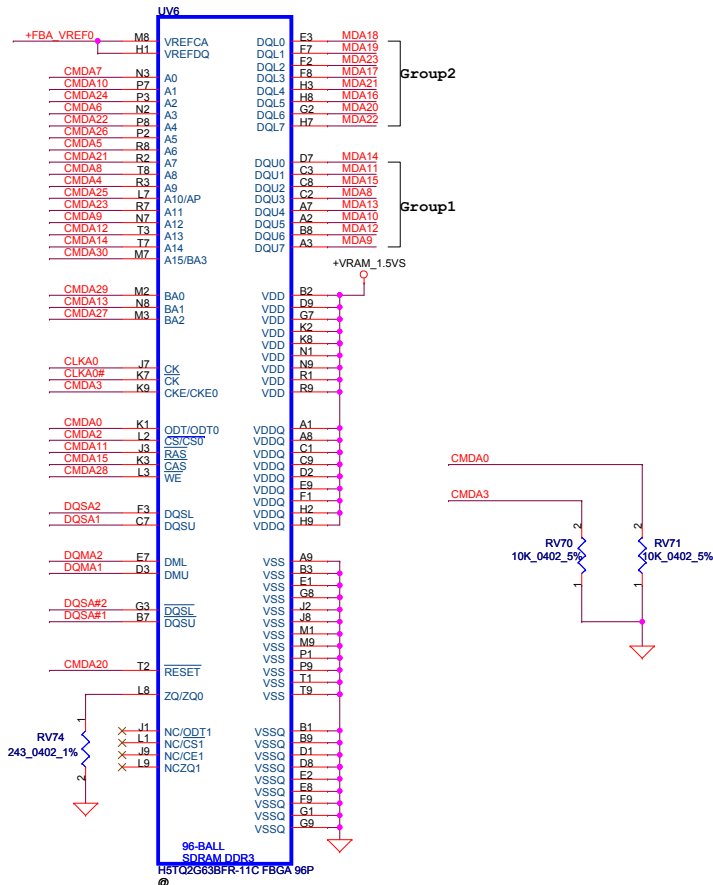
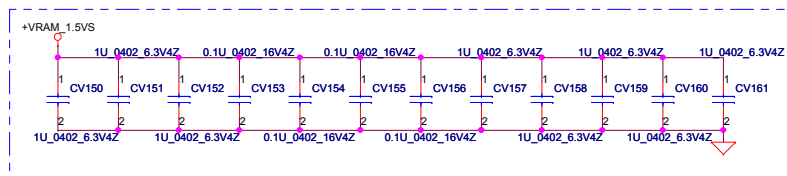
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



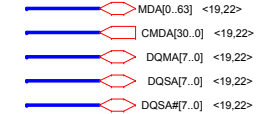
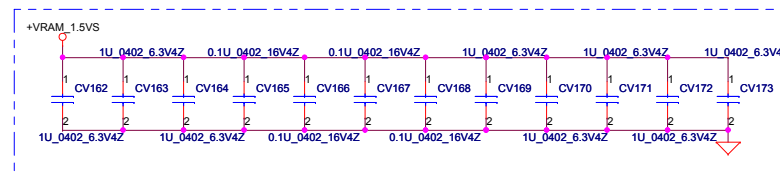
Support N12P-GV/GS
Support Max VRAM 2G



Under UV5 (below 150mils)



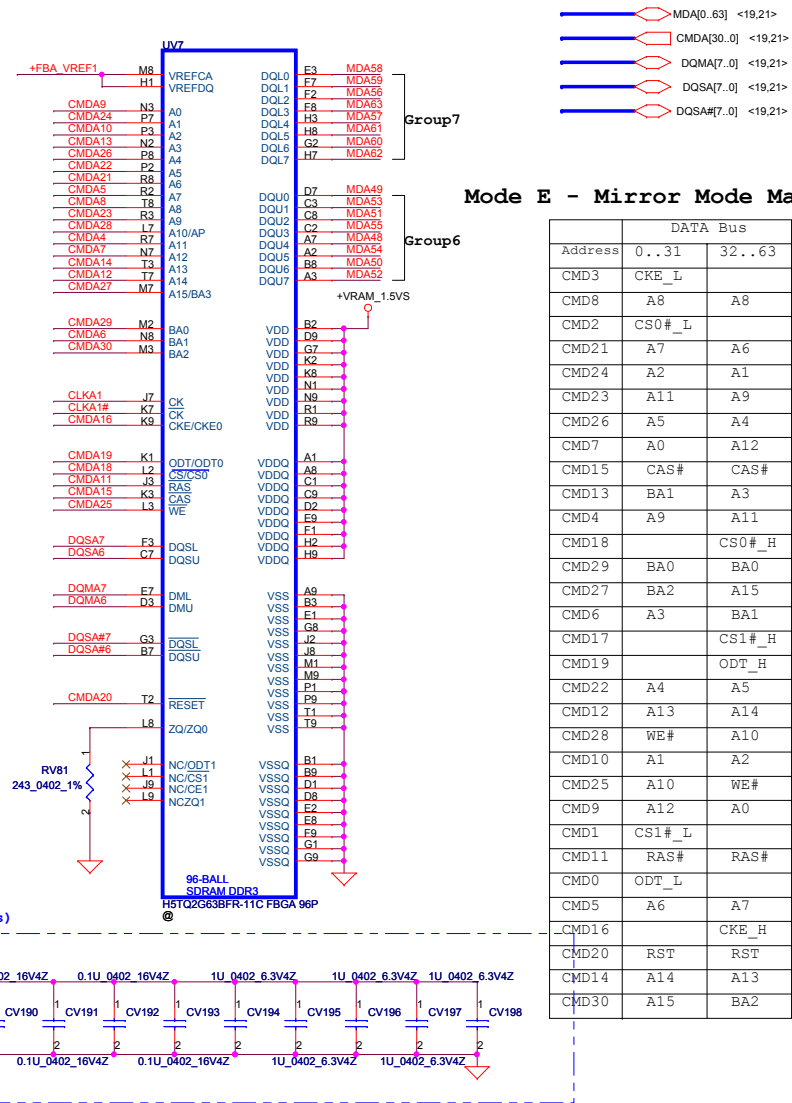
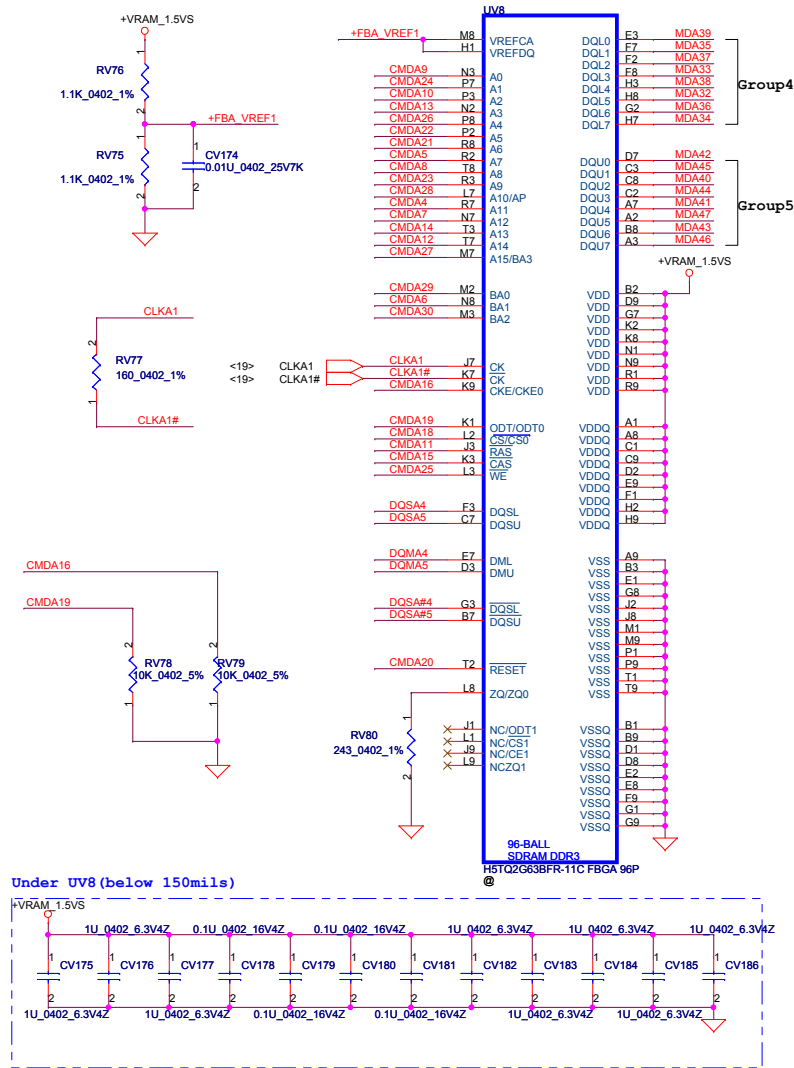
Under UV6 (below 150mils)



Mode E - Mirror
Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

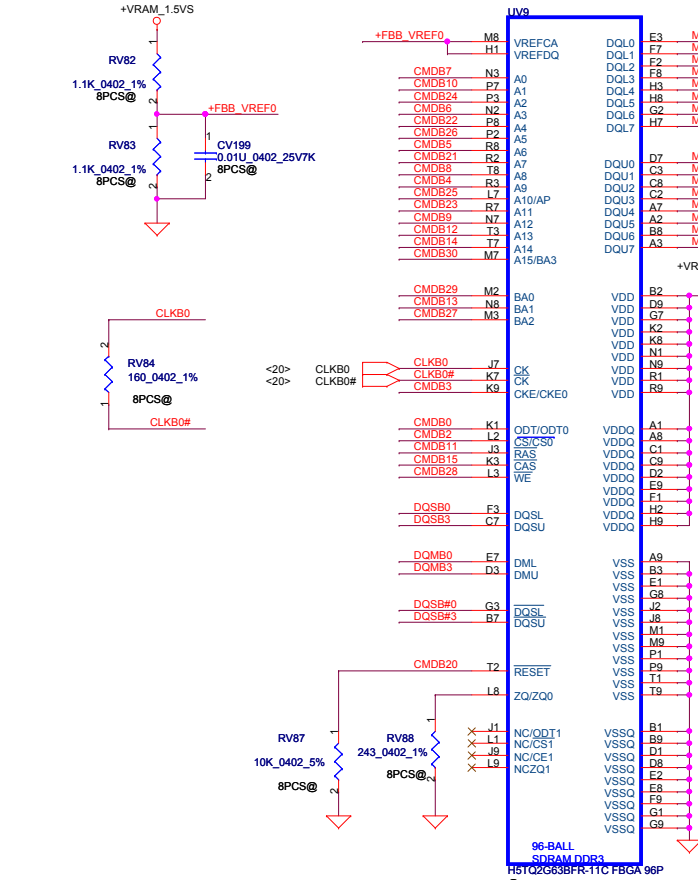
Memory Partition A - Upper 32 bits



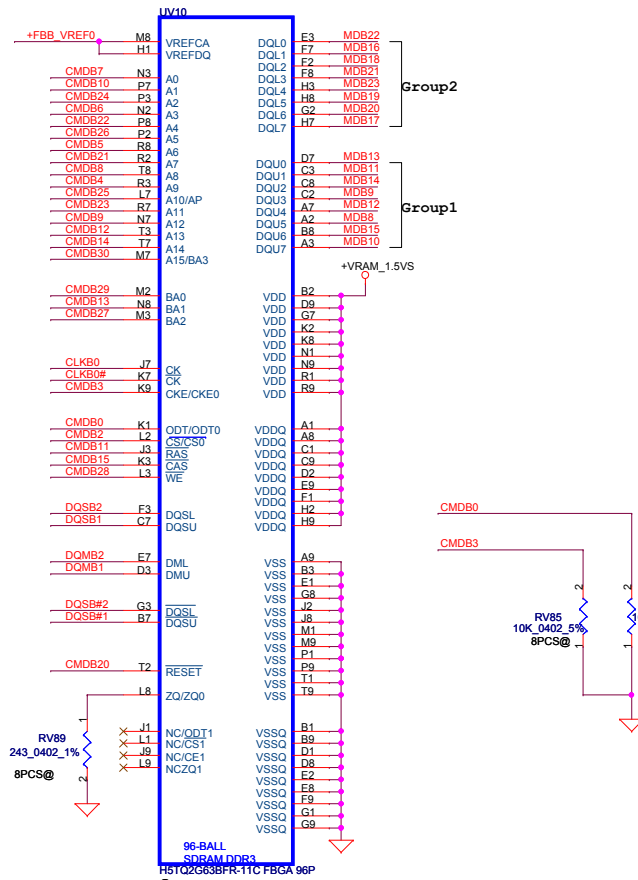
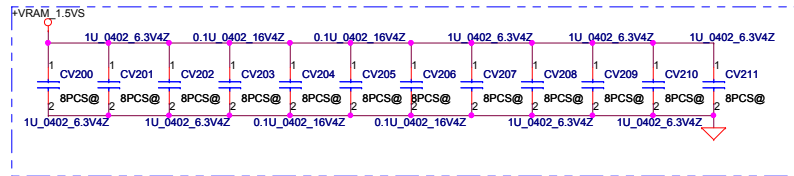
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

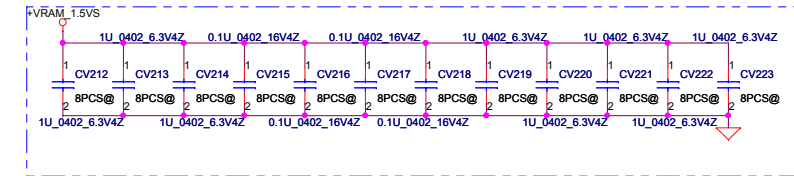
Memory Partition C - Lower 32 bits



Under UV9 (below 150mils)



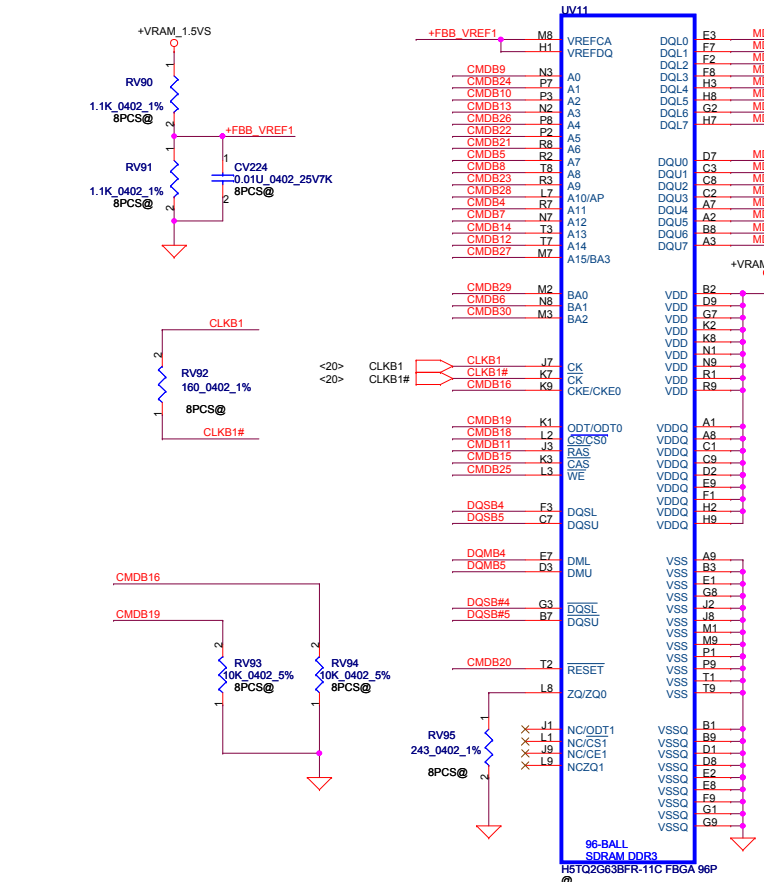
Under UV10 (below 150mils)



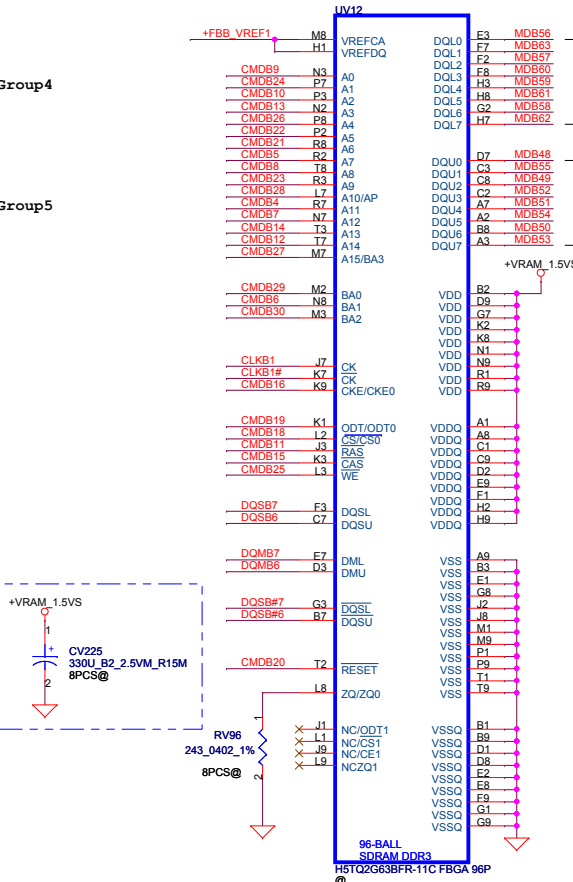
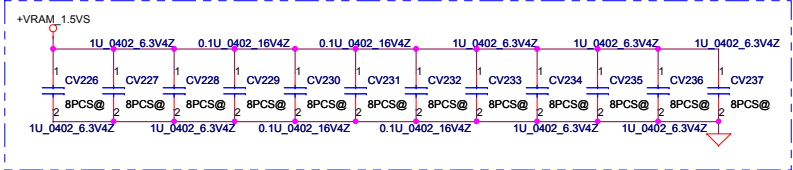
Mode E - Mirror Mode Mapping

Address		DATA Bus	
Address	0..31	32..63	
CMD3	CKE_L		
CMD8	A8	A8	
CMD2	CS0#_L		
CMD21	A7	A6	
CMD24	A2	A1	
CMD23	A11	A9	
CMD26	A5	A4	
CMD7	A0	A12	
CMD15	CAS#	CAS#	
CMD13	BA1	A3	
CMD4	A9	A11	
CMD18		CS0#_H	
CMD29	BA0	BA0	
CMD27	BA2	A15	
CMD6	A3	BA1	
CMD17		CS1#_H	
CMD19		ODT_H	
CMD22	A4	A5	
CMD12	A13	A14	
CMD28	WE#	A10	
CMD10	A1	A2	
CMD25	A10	WE#	
CMD9	A12	A0	
CMD1	CS1#_L		
CMD11	RAS#	RAS#	
CMD0	ODT_L		
CMD5	A6	A7	
CMD16		CKE_H	
CMD20	RST	RST	
CMD14	A14	A13	
CMD30	A15	BA2	

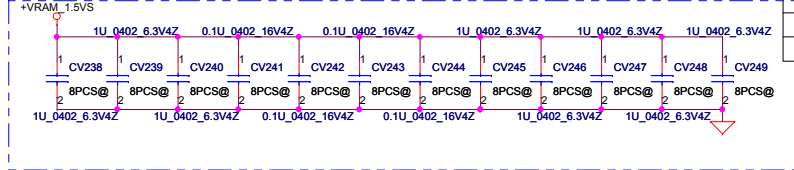
Memory Partition C - Upper 32 bits



Under UV11(below 150mils)



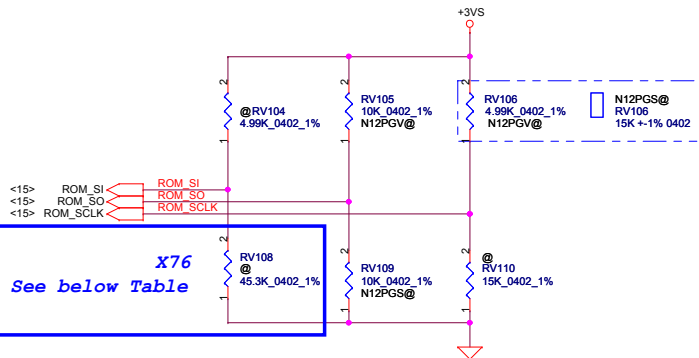
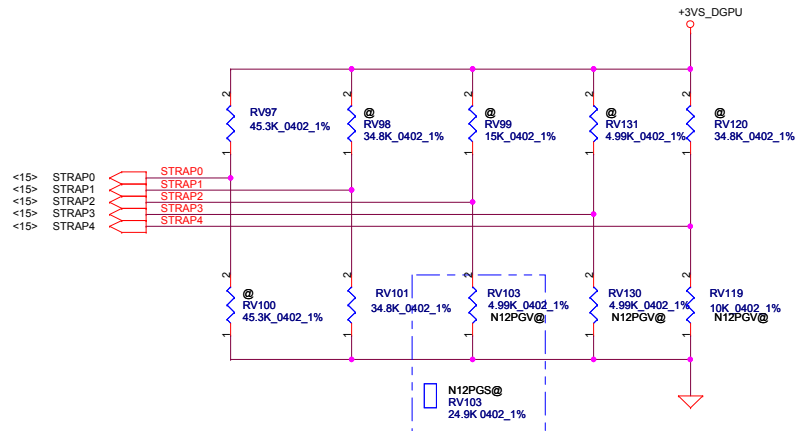
Under UV12(below 150mils)



- MDB[0..63] <20,23>
- CMDDB[30..0] <20,23>
- DOMB[7..0] <20,23>
- DQSB[7..0] <20,23>
- DQSB# [7..0] <20,23>

Mode E - Mirror Mode Mapping

DATA Bus	
Address	
CMD3	0..31 32..63
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT#_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT#_L
CMD5	A6
CMD16	CKE#_H
CMD20	RST
CMD14	A14
CMD30	A15



GPU	DeviceID	ROM_SI	ROM_SCLK	ROM_SO	STRAP0
N12P-GS	0x0DF4	Below Table	Pull up 15K	Pull down 10K	Pull up 45K
N12P-GV	0x1050	Below Table	Pull up 5K	Pull up 10K	Pull up 45K

GPU	DeviceID	STRAP1	STRAP2	STRAP3	STRAP4
N12P-GS	0x0DF4	Pull down 35K	Pull down 25K		
N12P-GV	0x1050	Pull down 35K	Pull down 5K	Pull down 5K	Pull down 10K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

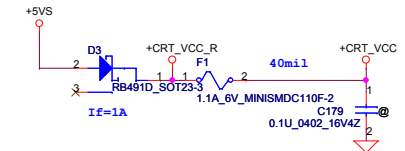
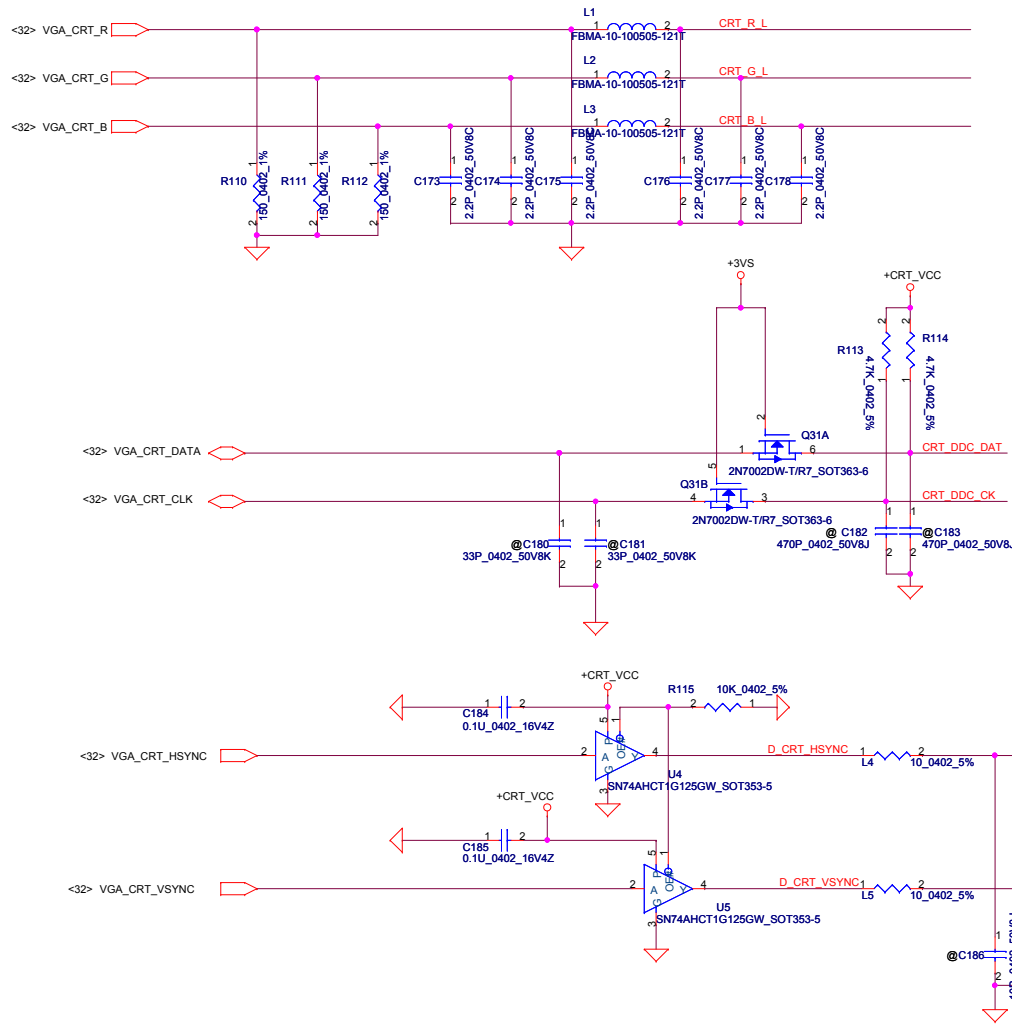
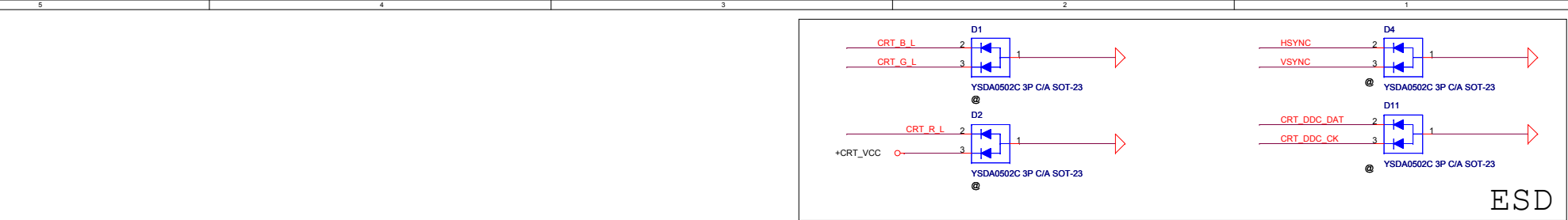
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

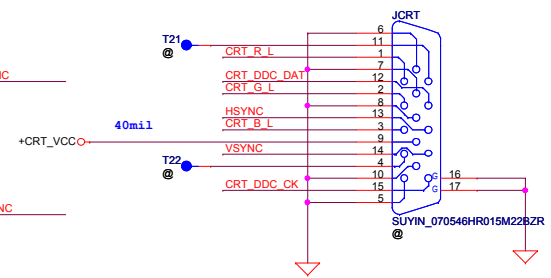
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

GPU	DDR3 Type	VRAM		RAMCFG[3..0]		RV108
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C	512MB	0010	PD 15K	SD034154280
		SA000041S20	1GB	0010	PD 15K	SD034154280
		Samsung K4W1G1646E-HC11	512MB	0011	PD 20K	SD034200280
		SA000041T00	1GB	0011	PD 20K	SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C	1GB	0110	PD 34.8K	SD034348280
		SA00003Y000	2GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC11	1GB	0111	PD 45.3K	SD034453280
		SA000047Q00	2GB	0111	PD 45.3K	SD034453280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C	512MB	0010	PD 15K	SD034154280
		SA0000324C0	512MB	0011	PD 20K	SD034200280
		Samsung K4W1G1646G-BC12				
		SA00004HS00	1GB	0110	PD 34.8K	SD034348280
	128M16 800MHz	Hynix H5TQ2G63BFR-12C				
		SA00003VS00				
Samsung K4W2G1646C-HC12						
SA00003MQ40		1GB	0111	PD 45.3K	SD034453280	

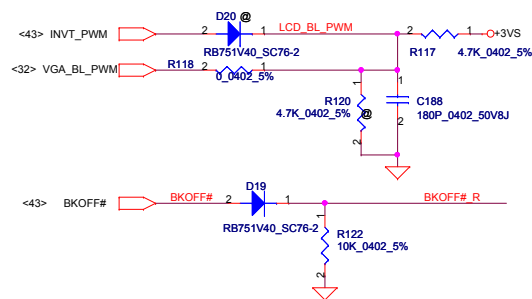
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Issued Date	2010/12/03	Deciphered Date	2011/12/03	Title	VGA(12/12)-MISC	
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					PBL80 LA-7441P M/B	0.1
				Date:	Friday, January 21, 2011	Sheet 25 of 58



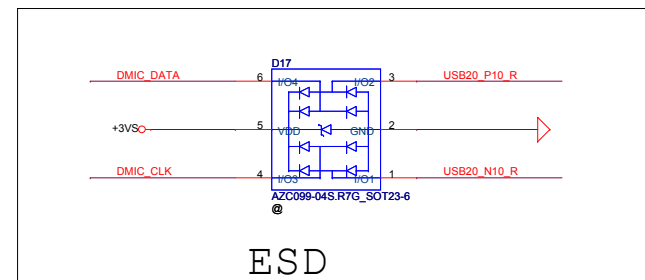
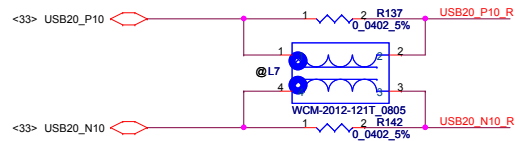
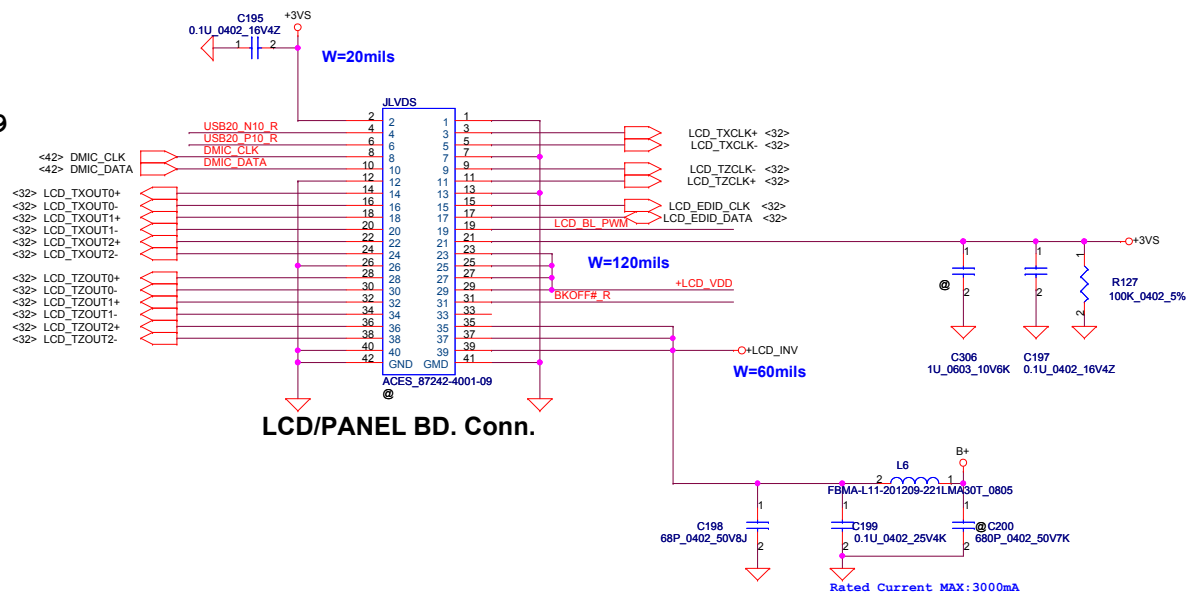
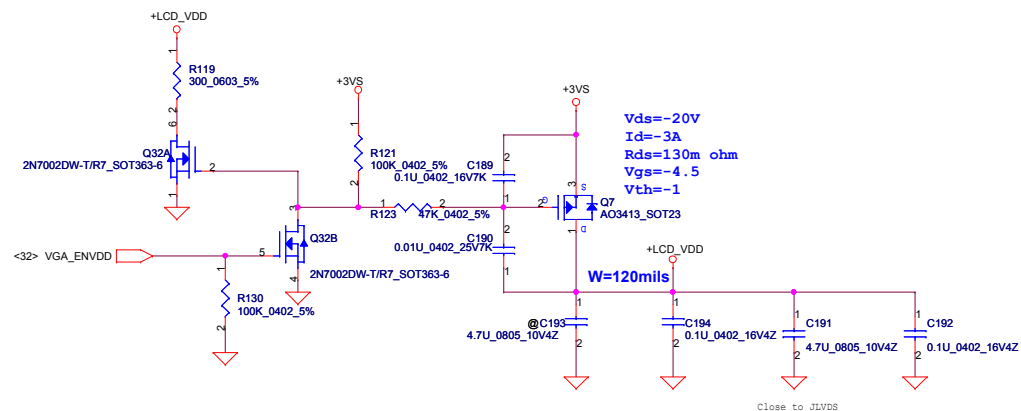
CRT CONNECTOR



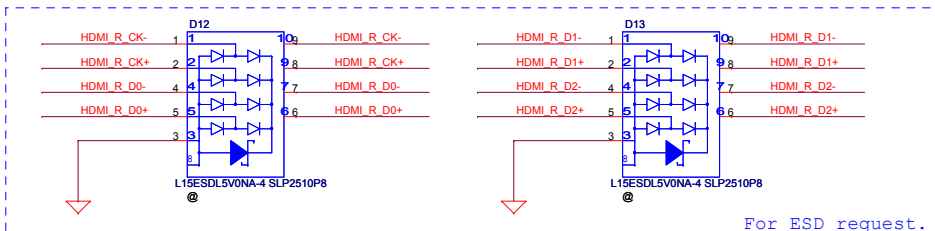
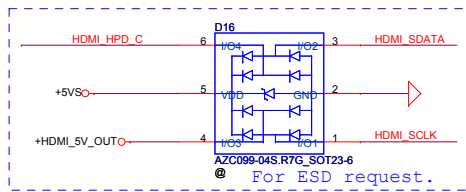
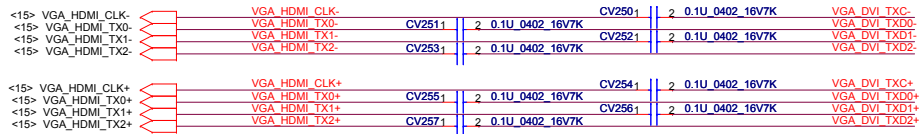
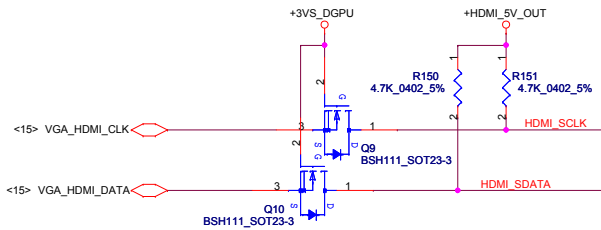
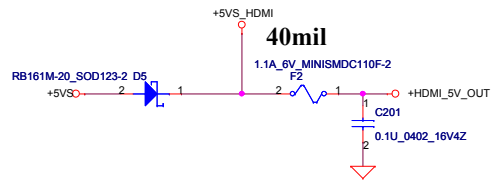
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/12/03	Deciphered Date	2011/12/03	Title	CRT
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					PBL80 LA-7441P M/B
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3		2		1	Sheet 26 of 58
					Rev 0.1



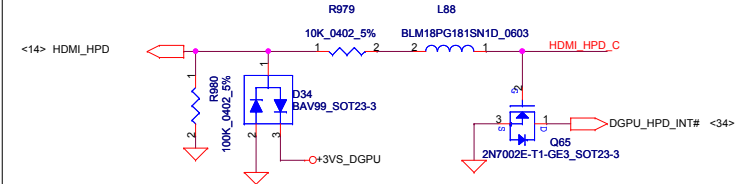
Dual Channel LVDS Support 18.4" HD/FHD 16:9



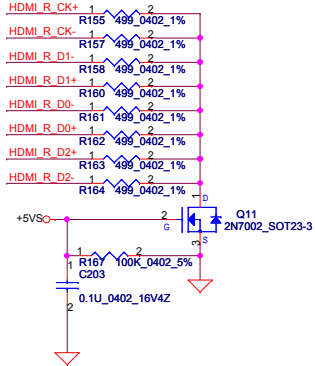
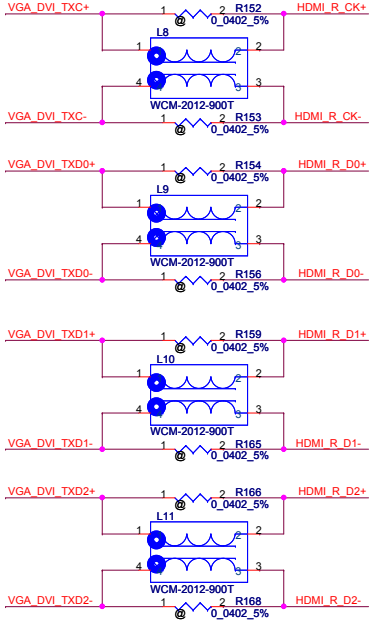
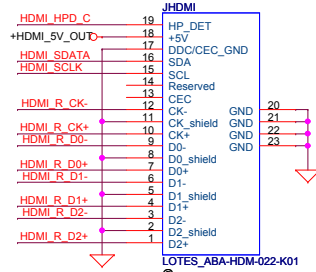
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				Document Number	
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				0.1	
				Date	
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				Sheet	
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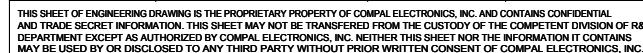
NV review, request for LC filter at HPD at 12/17.

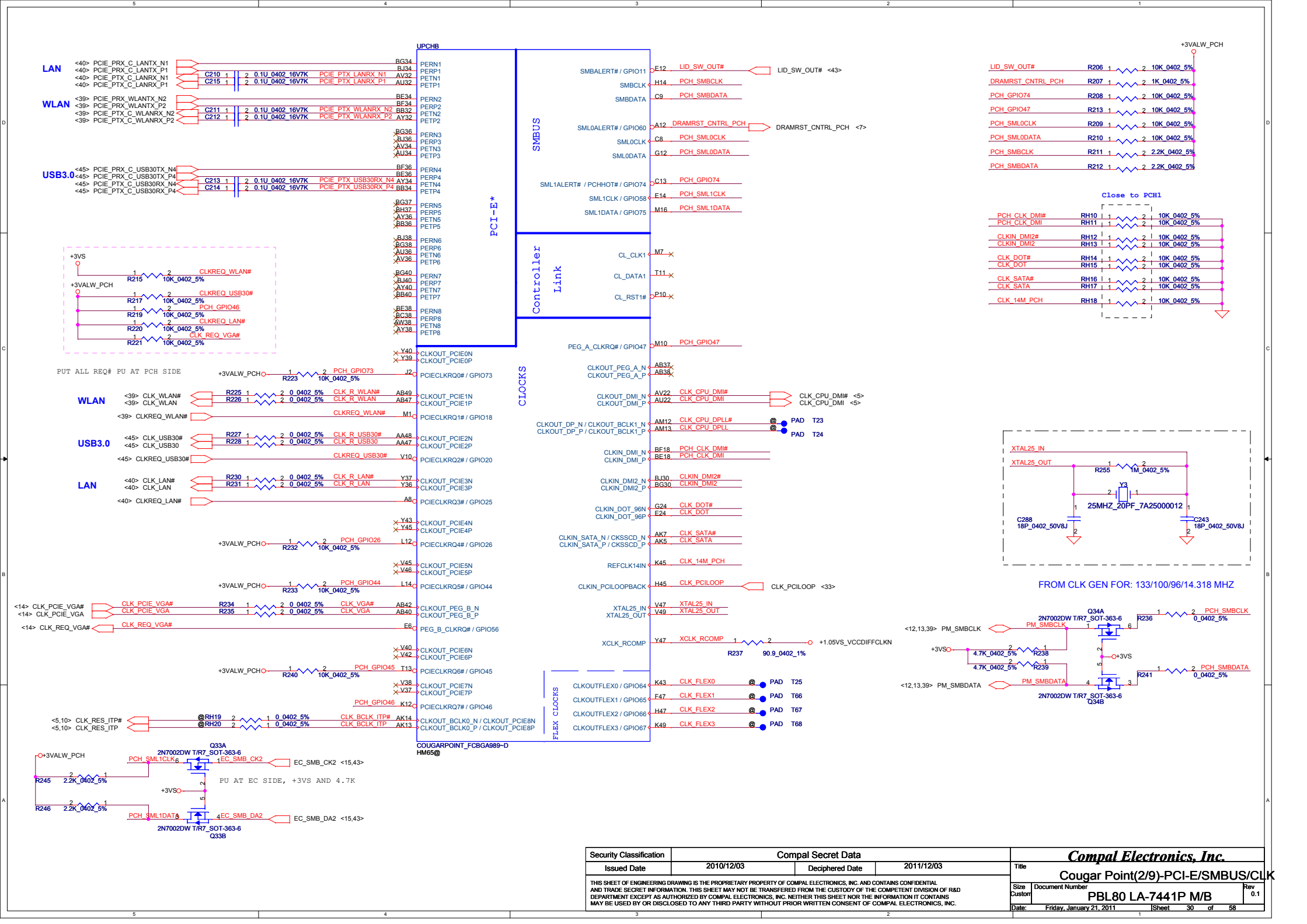


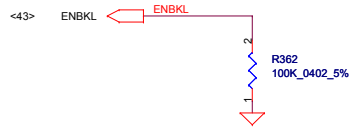
HDMI Connector



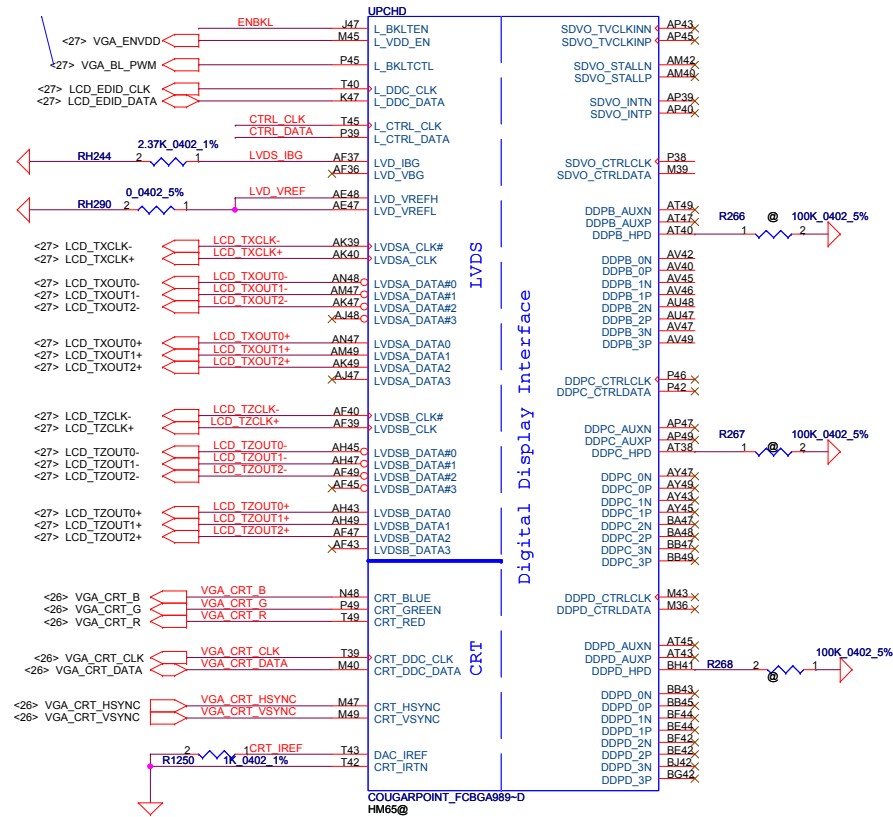
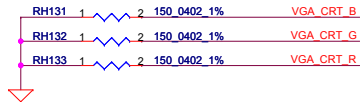
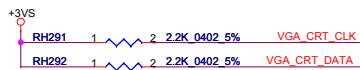
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/12/03	Deciphered Date	2011/12/03	Title	
				HDMI Connector	
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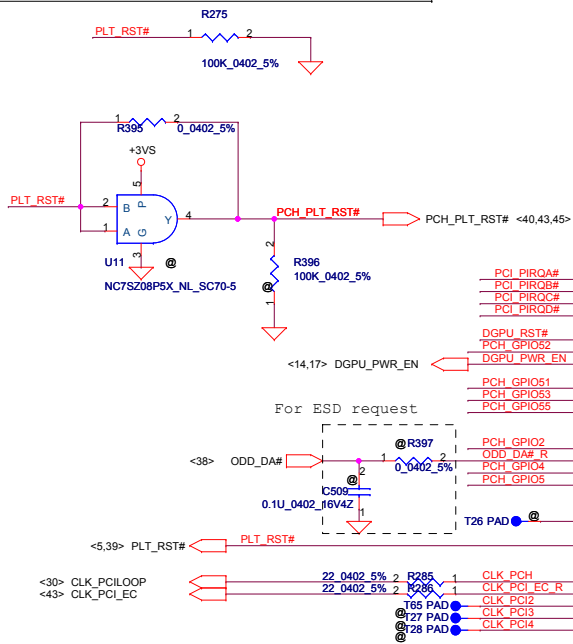
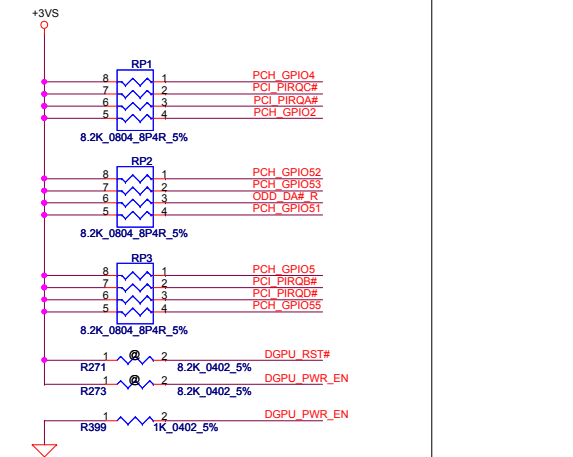




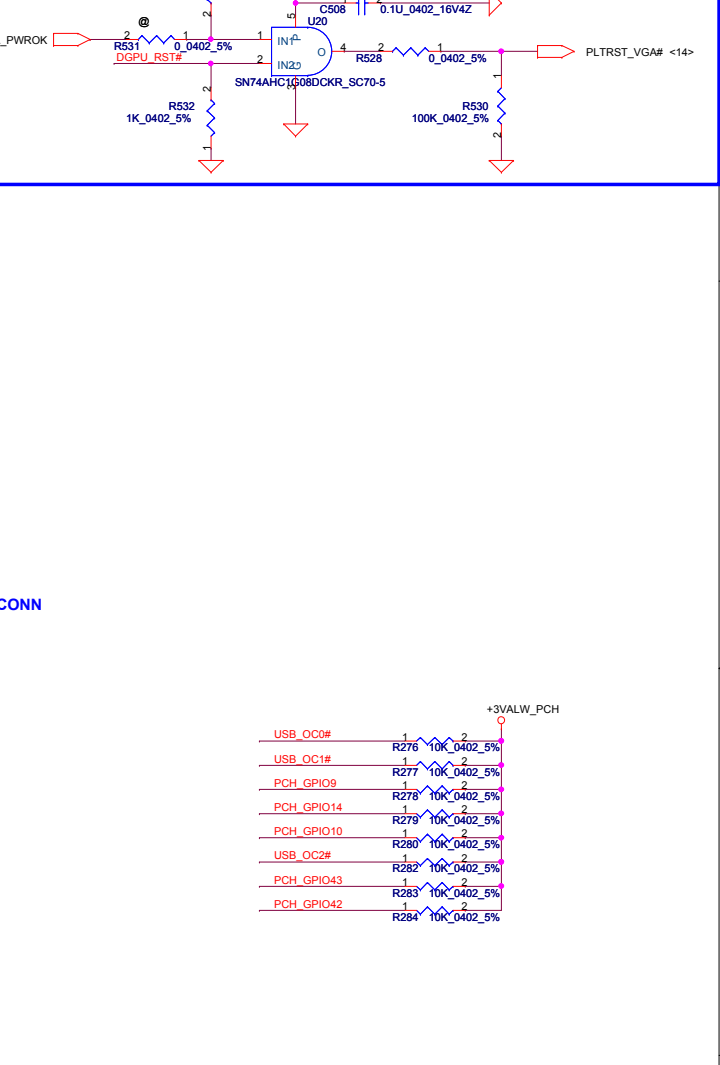
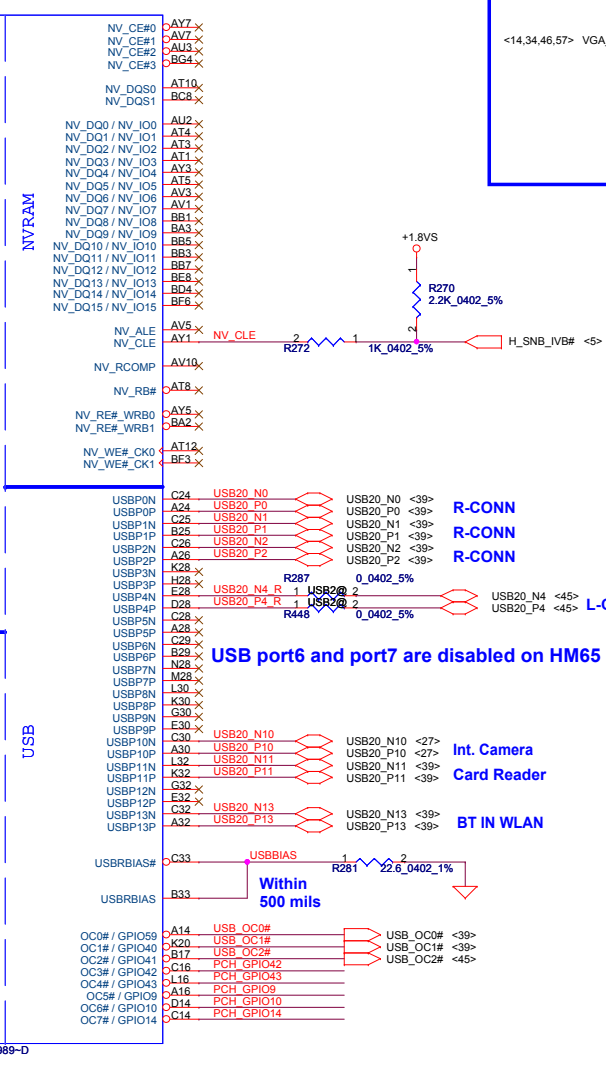
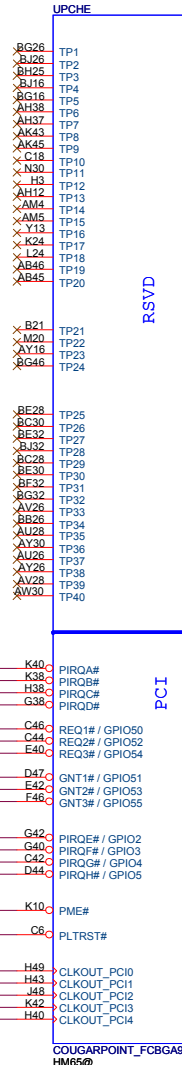
Pull high at LVDS conn side.

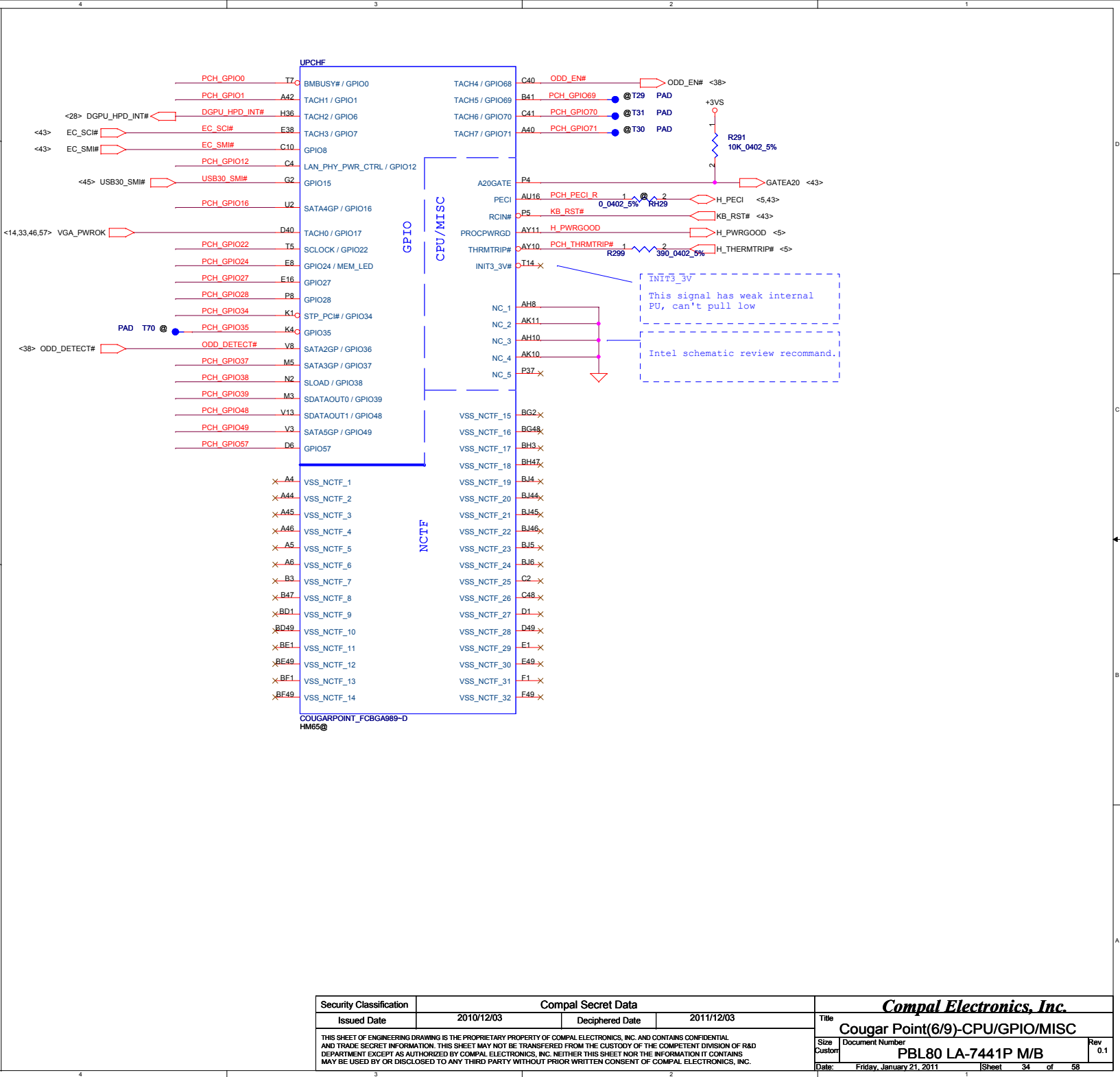
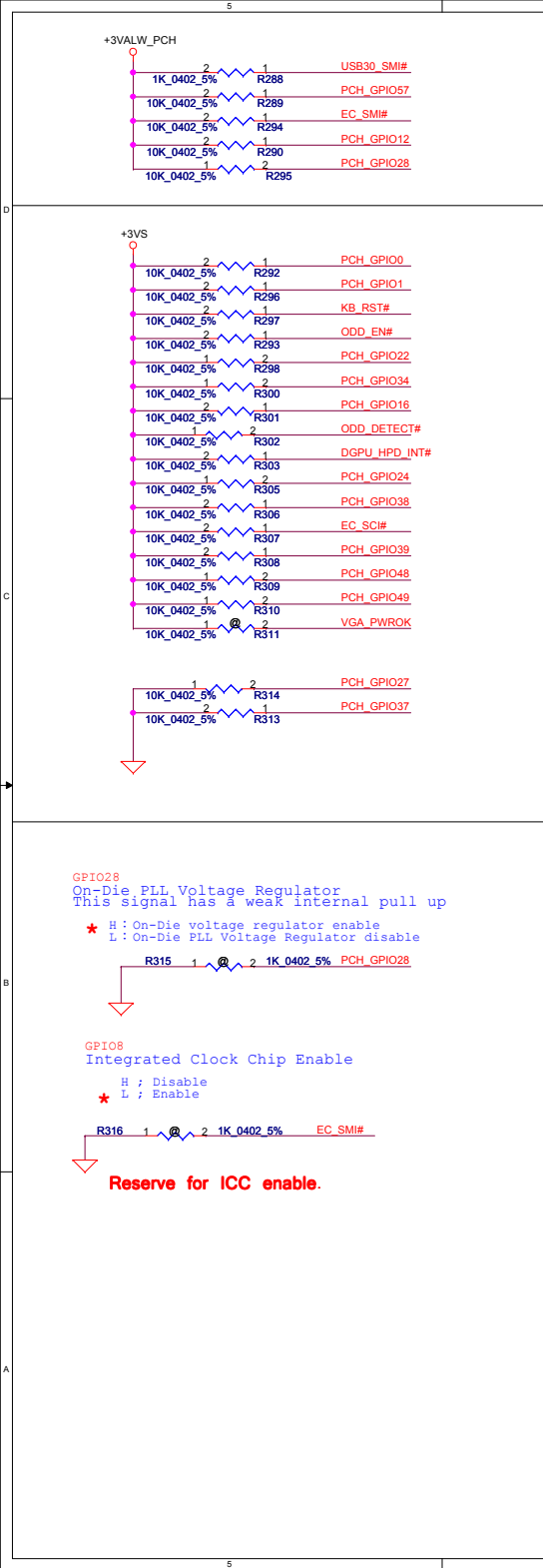


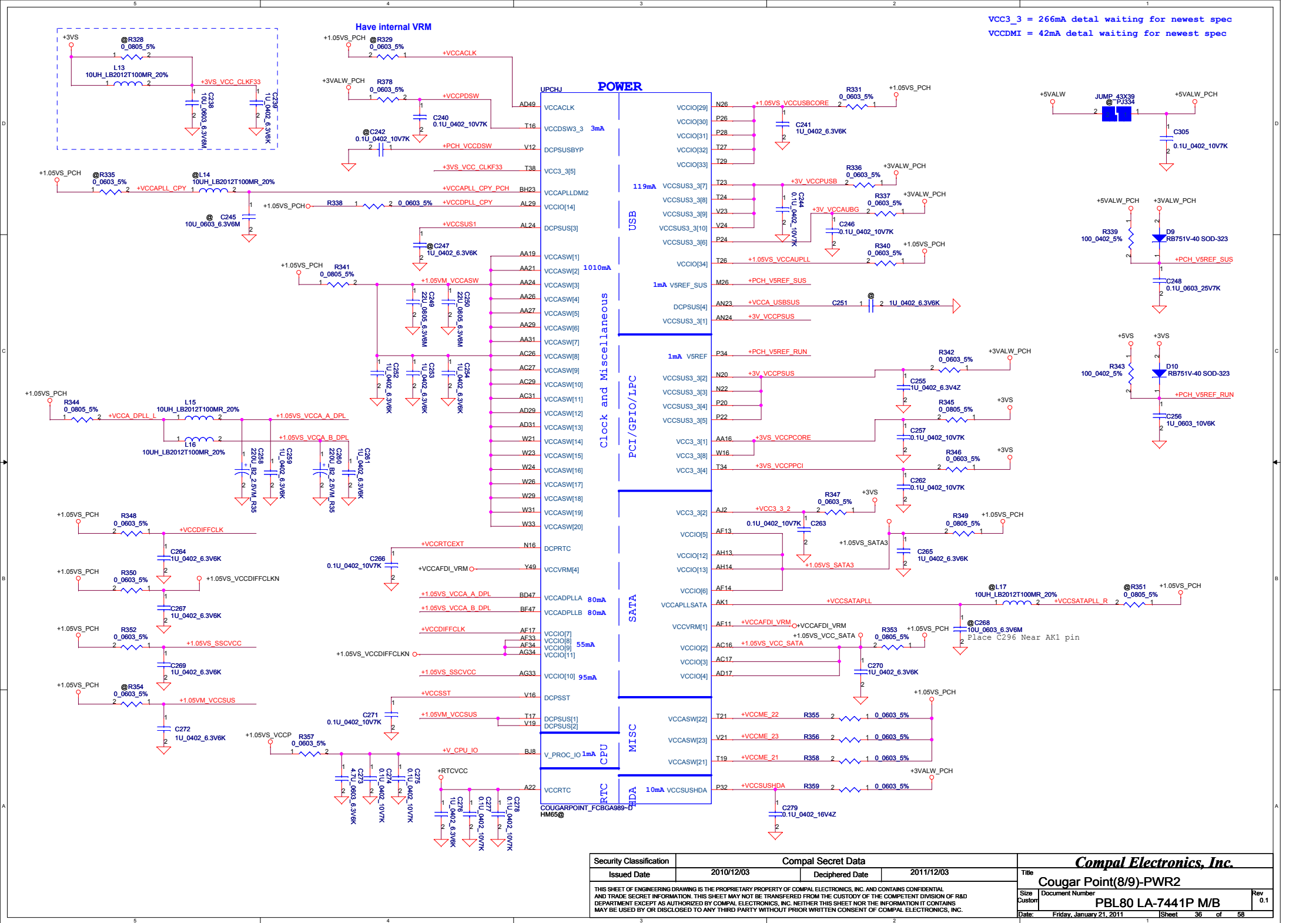
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				Custon	PBL80 LA-7441P M/B
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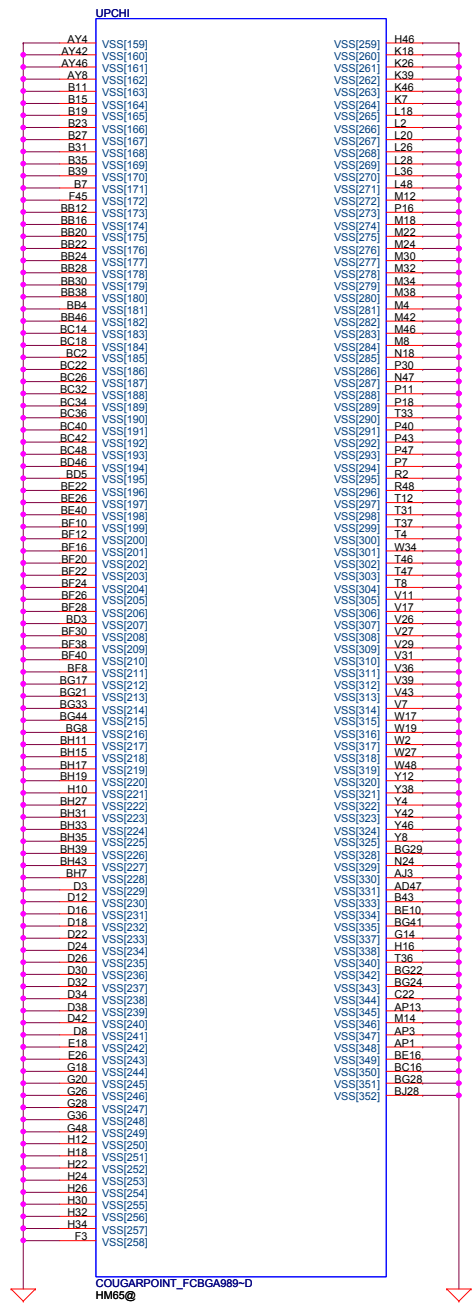
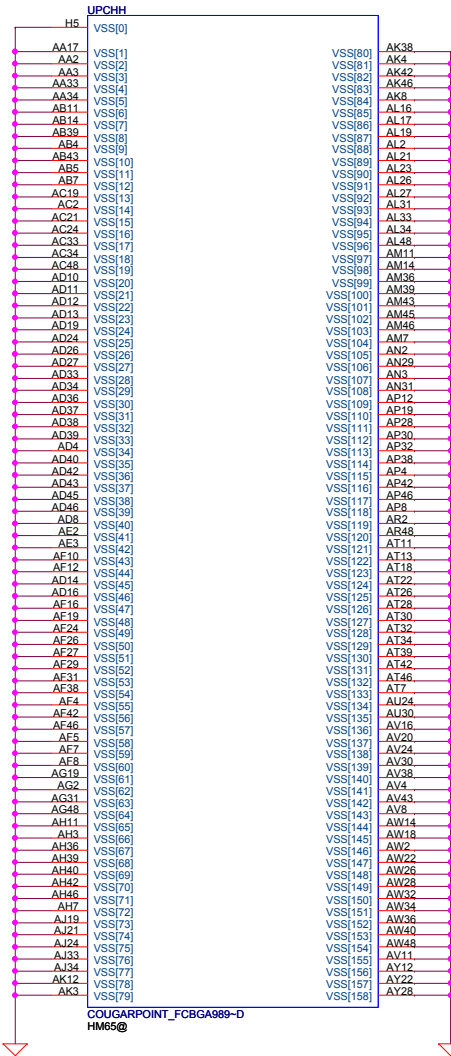


Boot BIOS Strap bit1 BBS1		
	Bit11	Bit10
GNT1#/ GPIO51	0	1
	1	0
	1	1
	0	0

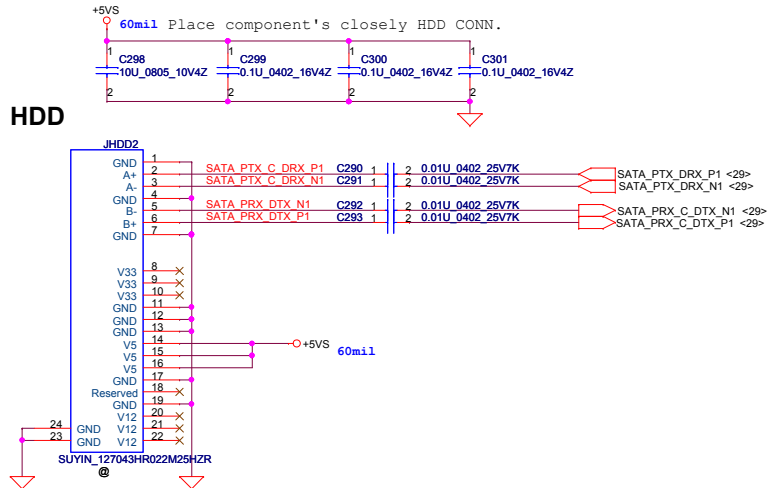




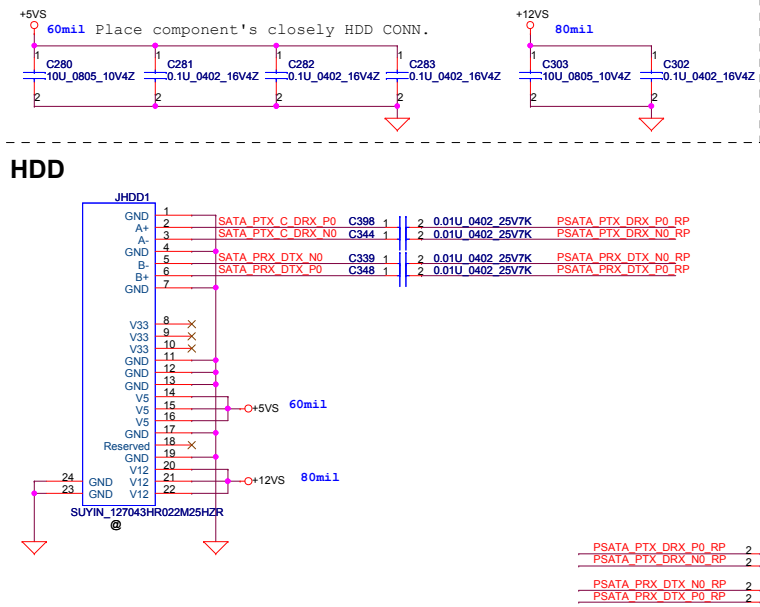




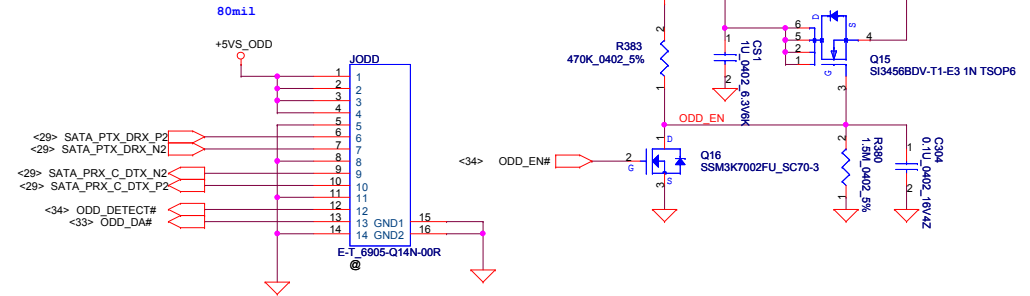
SATA HDD 2.5" Conn.



SATA HDD 3.5" Conn.

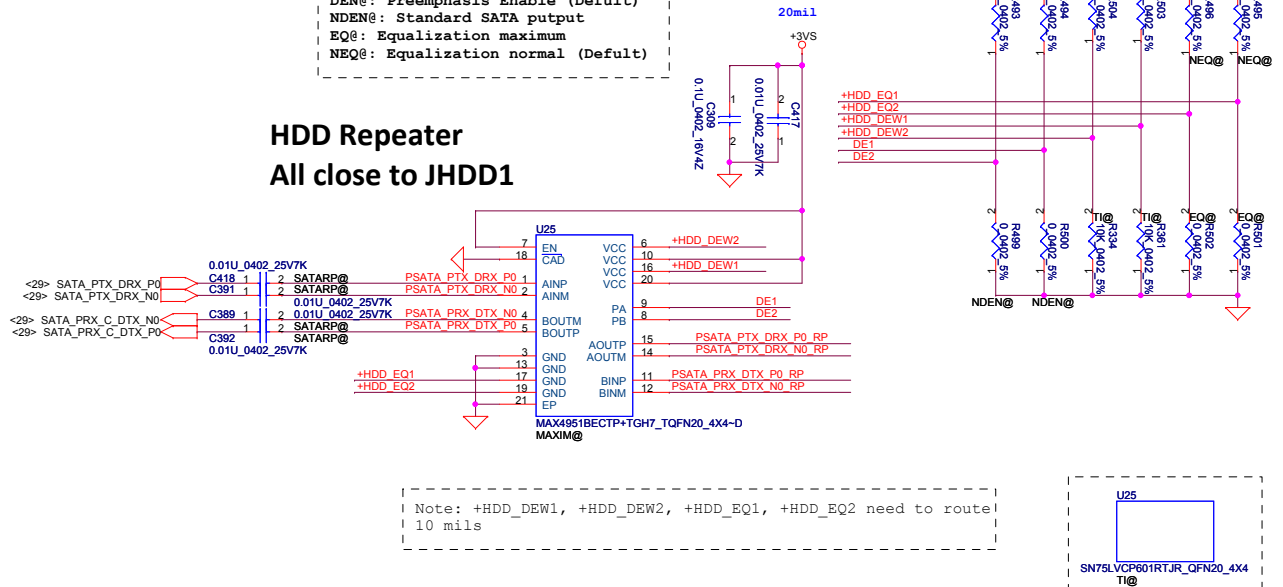


ODD small board conn



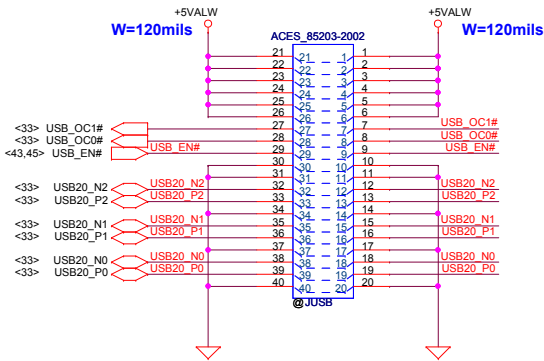
```
MAXIM@: MAX4951BECTP+TGH7 (Default)
TI@: SN75LVCP601TJR
DEN@: Preemphasis Enable (Default)
NDEN@: Standard SATA putput
EQ@: Equalization maximum
NEQ@: Equalization normal (Default)
```

HDD Repeater
All close to JHDD1

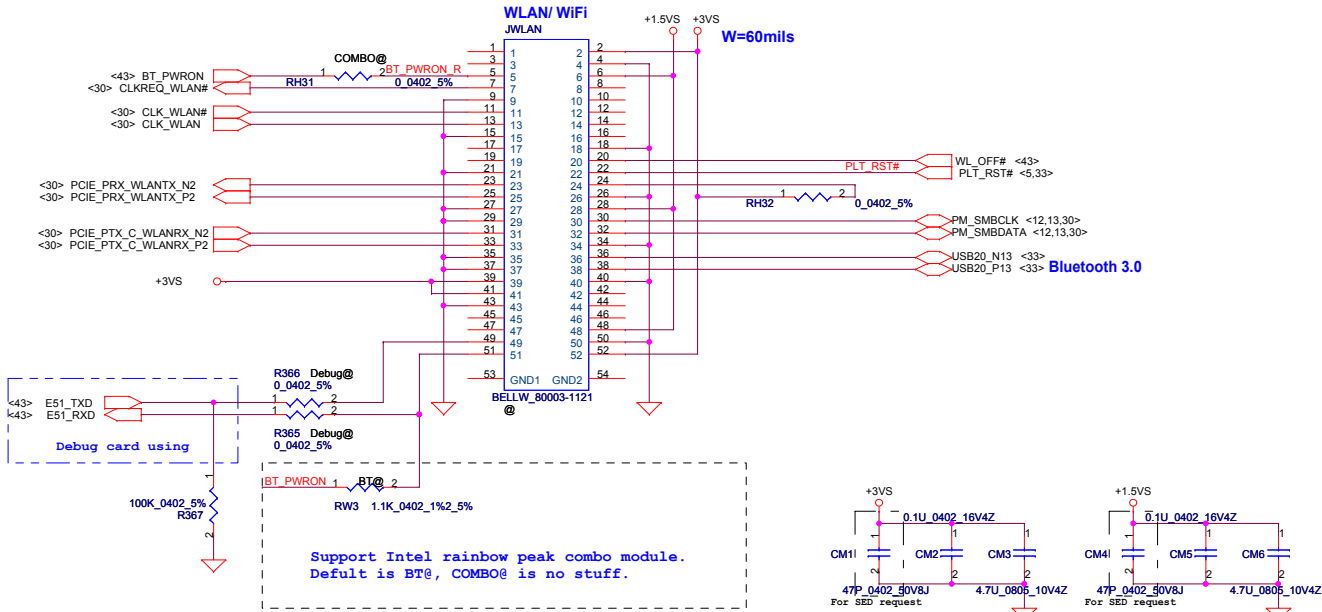


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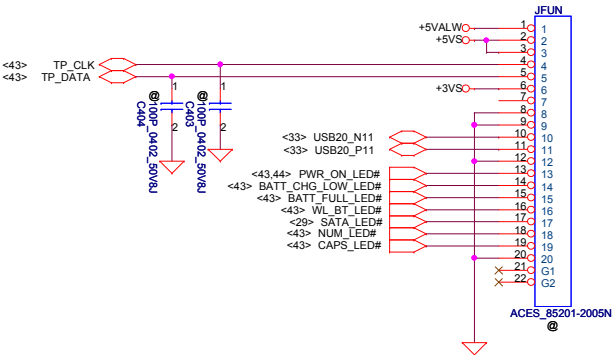
USB/B
Right USB X 3



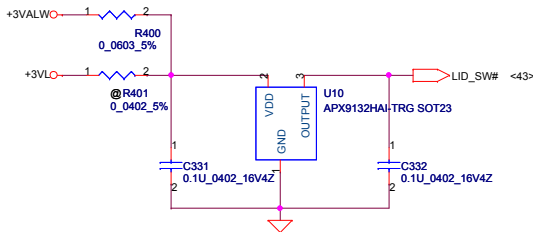
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



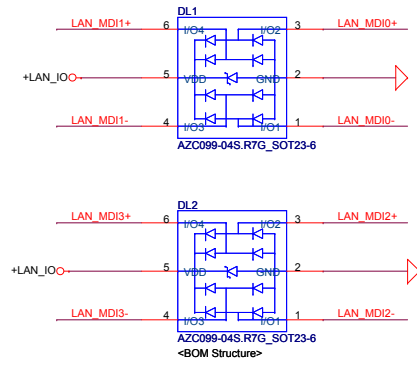
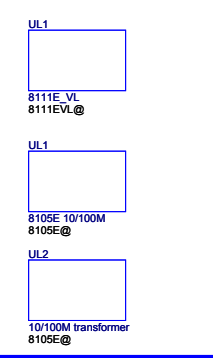
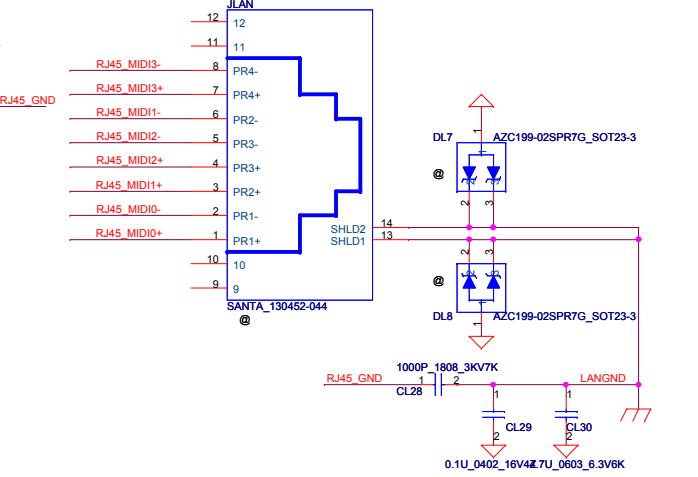
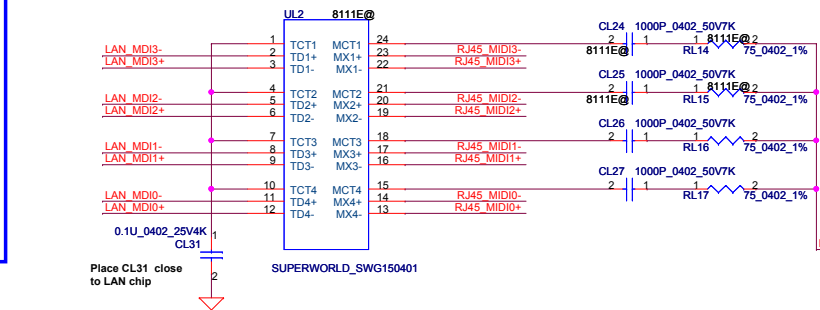
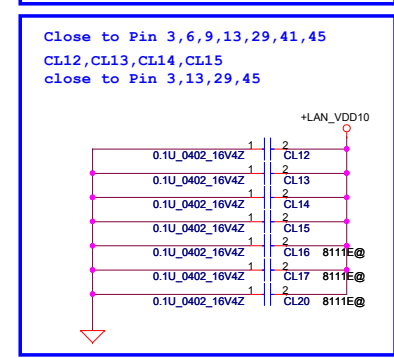
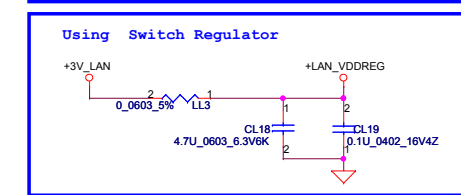
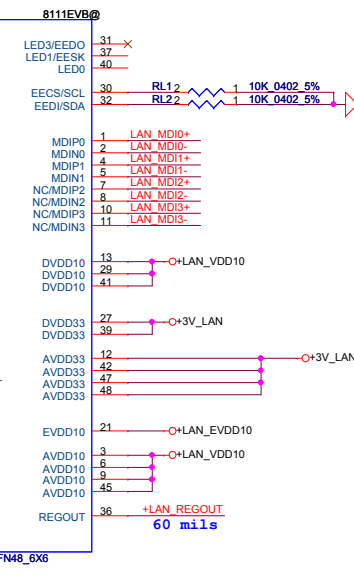
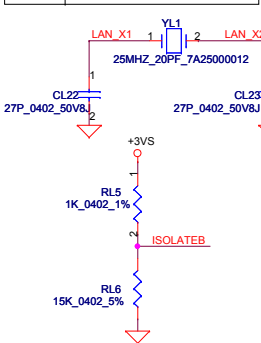
Touch pad & LID &
Card Reader & LED small board Connector



Lid SW



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				USB/B&TP/LED/CR/B&LID&PCIe-WLAN	
				Size	Document Number
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BIOS Bus switch

SPI ROM For Basic ME ROM size

4MByte

1. When Flash EC ROM.

KSO2 to Low (Test mode)

KSO3 to Low (ISP mode)-----FDA mode

EC_ON->Low, BUS_EN#->Low

U11 : Y->A0, PCH to BIOS ROM.

KSI4,5,6,7 direct to EC_SPI
2. When Flash BIOS ROM.

KSO2 to High

KSO3 to Low (ISP mode)

EC_ON->High, BUS_EN#->High.

U11 : Y->A1, KSI4,5,6,7 to BIOS ROM.

+3V_SPI from +3VALW

Set EC pin KSI4,5,6,7 to HiZ.
3. When normal operation.

EC_ON->High , BUS_EN#->Low.

U11 : Y->A0, PCH direct to BIOS ROM.

+3V_SPI from +3VS.
4. When enter S3,4

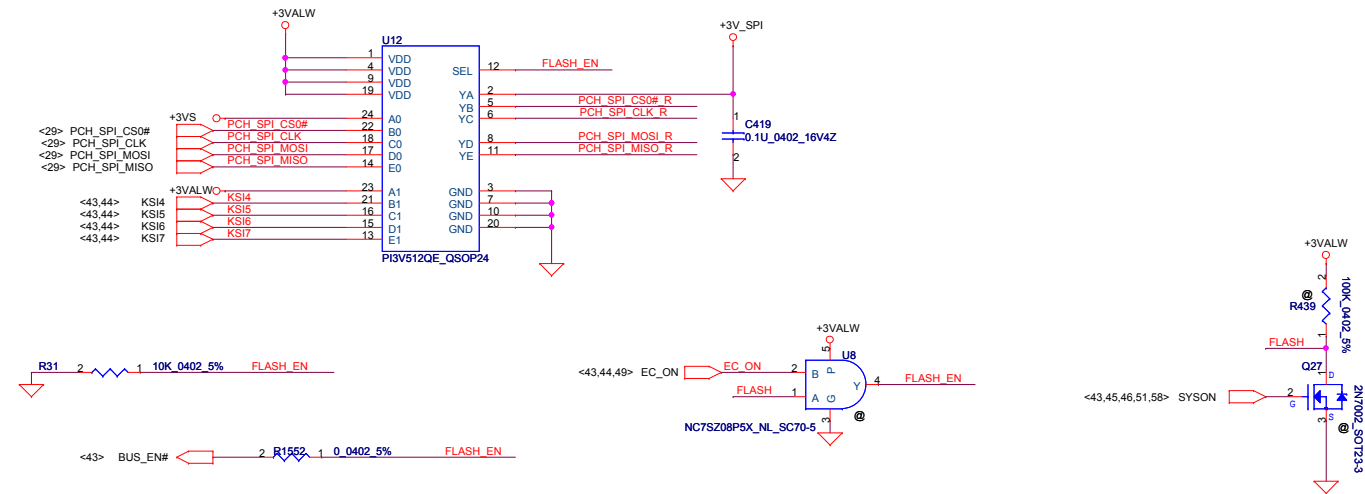
EC_ON->High, BUS_EN#->Low.

U11 : Y->A1, PCH direct to BIOS ROM.

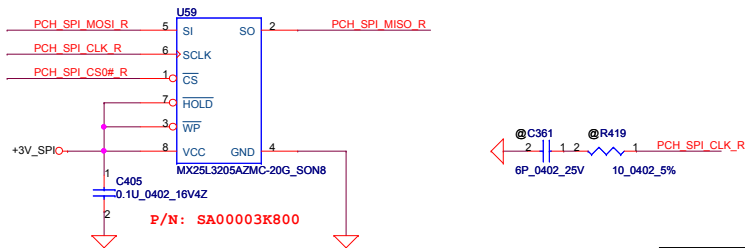
But +3V_SPI from +3VS is no power.
- ** BUS_EN# only high when test mode.

And must make sure it's low when FDA mode.

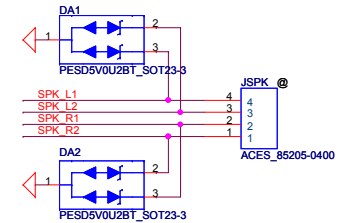
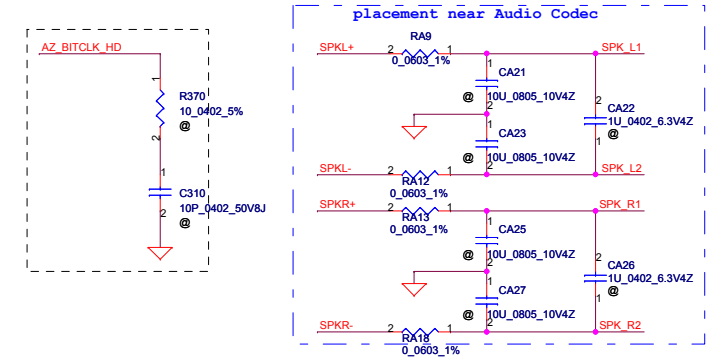
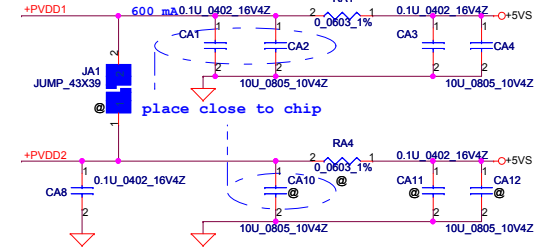
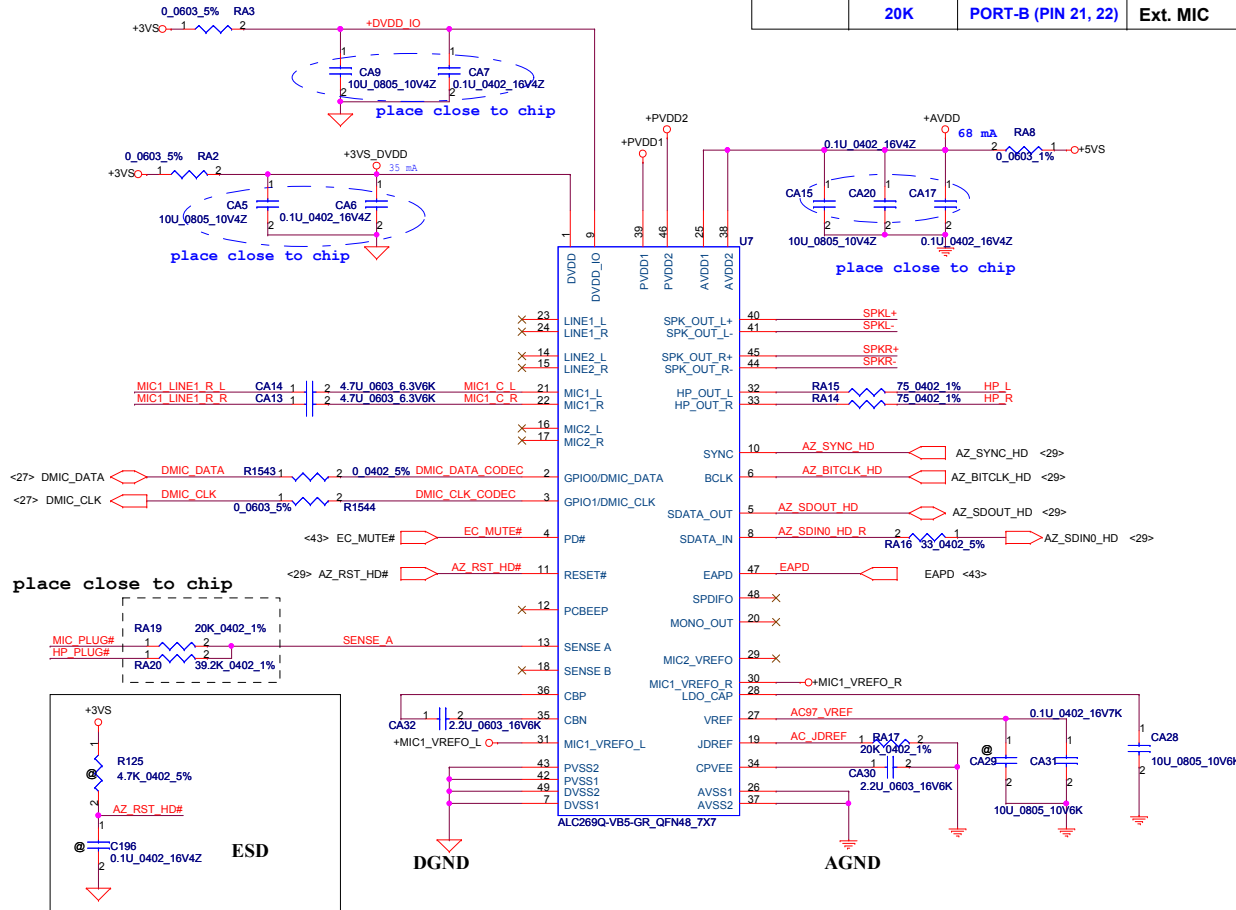
Or HW use 10K pull down to GND.



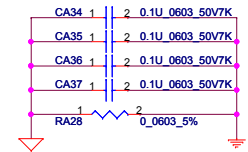
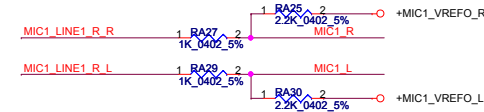
BIOS SPI Flash (4MByte*1)



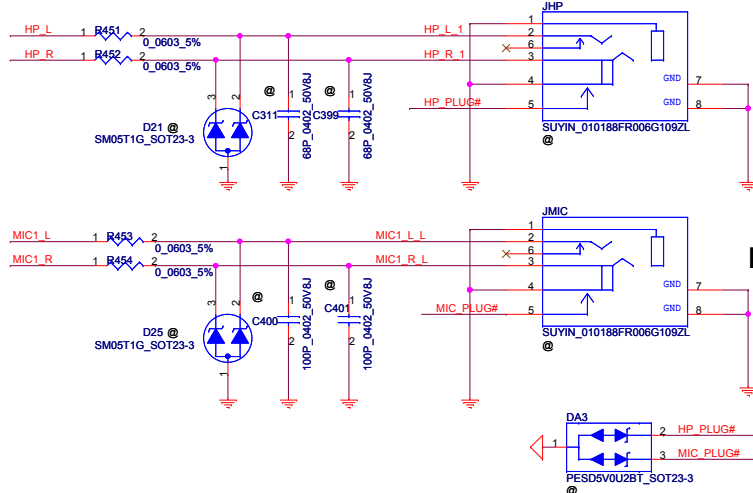
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC



Ext.MIC/LINE IN JACK

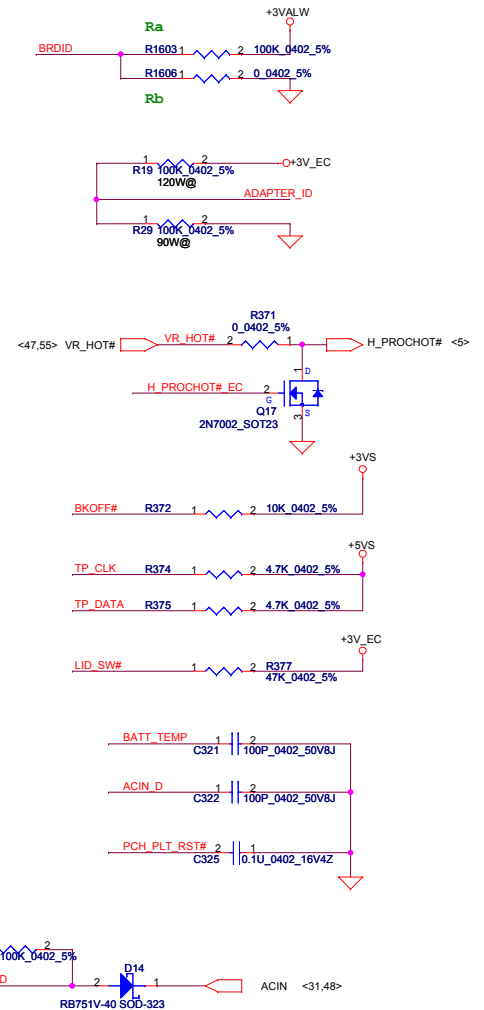
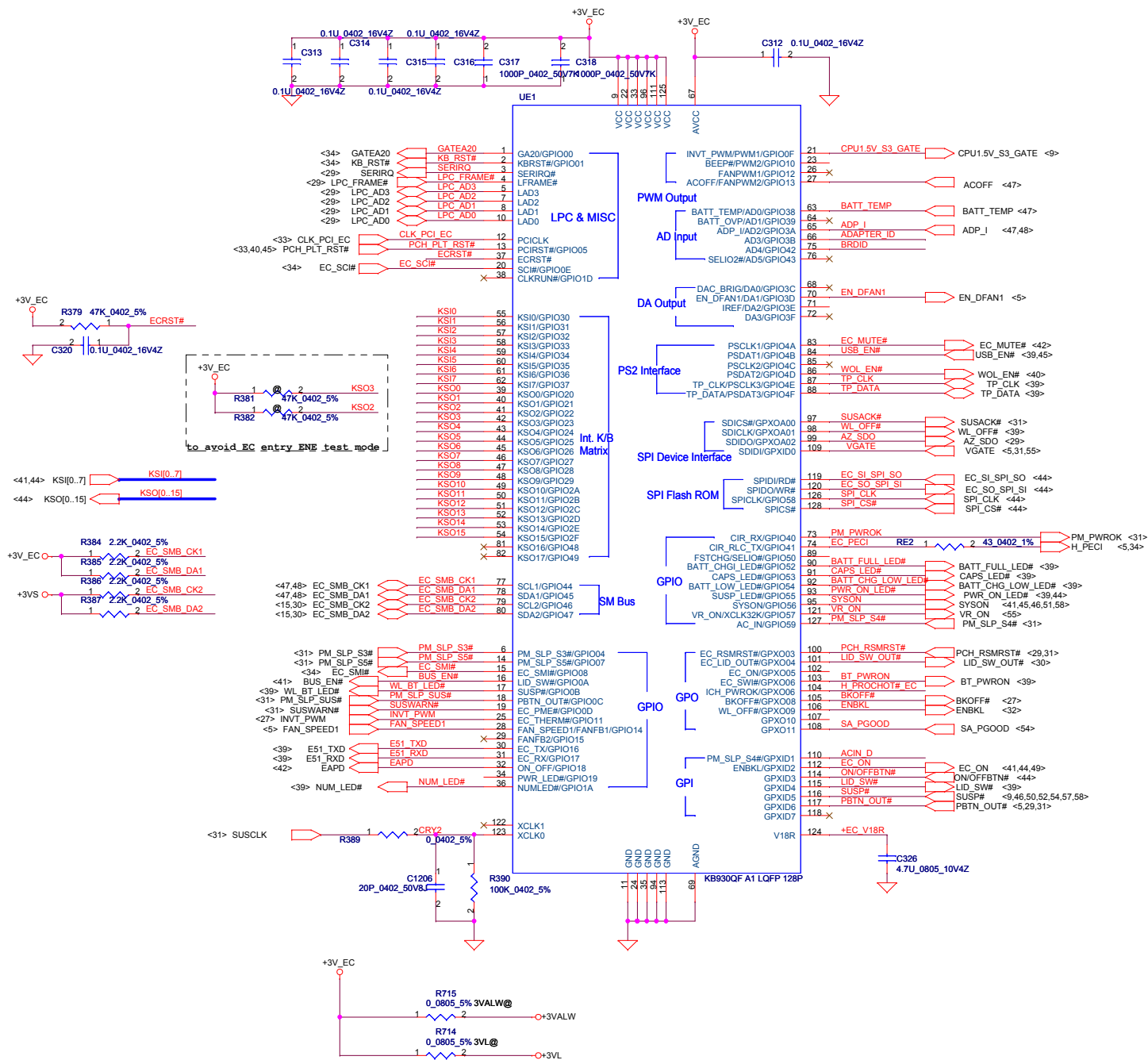


HP CONN & MIC CONN



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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V



EC Power : +3VALW(default)

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P/N : SA00003GK00 & SA00003GM10

Pinout diagram for the ACES_85201-24051 connector. The diagram shows a 24-pin connector with pins numbered 1 to 24. Pins 1 through 23 are labeled with KSO10 through KSO9, and pin 24 is labeled KSO9. The pins are connected to a 24-pin connector labeled JKB. The connections are as follows:

Pin	Label	Connector Pin
1	KSO10	1
2	KSO11	2
3	KSO12	3
4	KSO15	4
5	KSI7	5
6	KSI2	6
7	KSI3	7
8	KSI4	8
9	KSI0	9
10	KSI5	10
11	KSI6	11
12	KSI1	12
13	KSO2	13
14	KSO1	14
15	KSO0	15
16	KSO4	16
17	KSO3	17
18	KSO5	18
19	KSO6	19
20	KSO11	20
21	KSO10	21
22	KSO12	22
23	KSO14	23
24	KSO9	24

A ground symbol is shown at the bottom right, labeled GND1 and GND2.

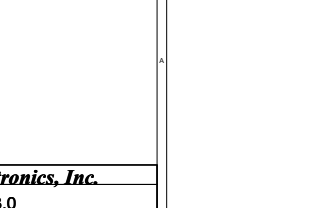
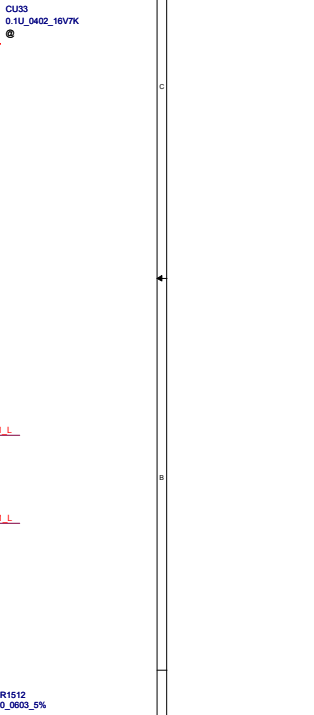
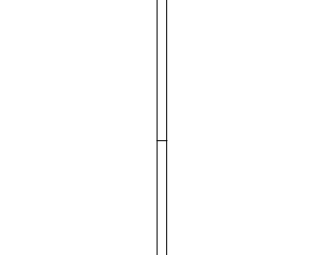
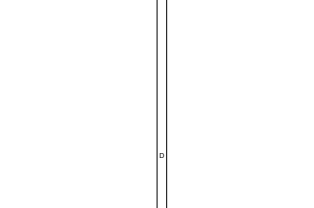
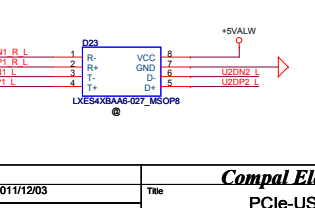
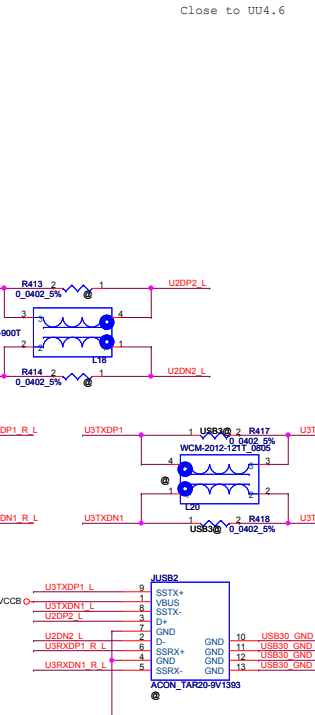
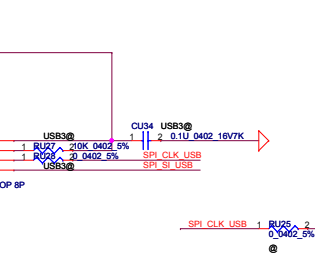
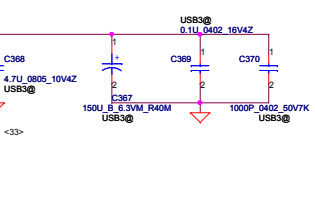
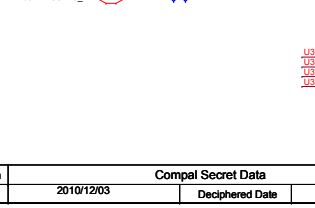
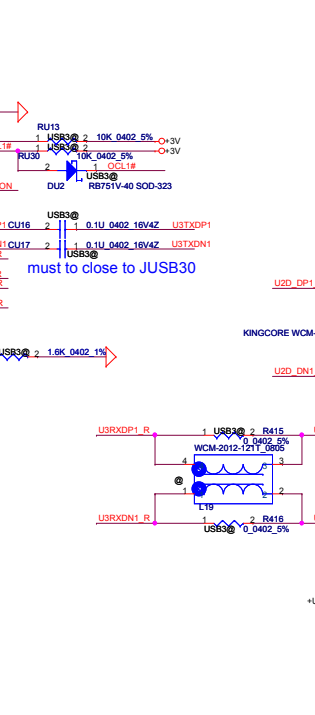
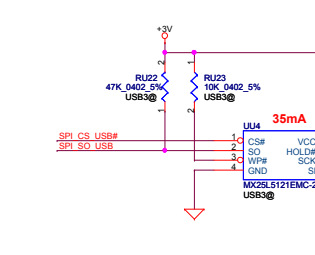
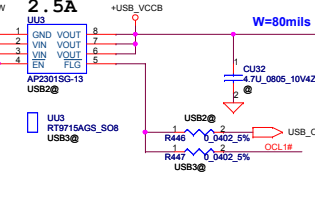
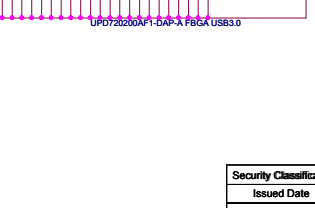
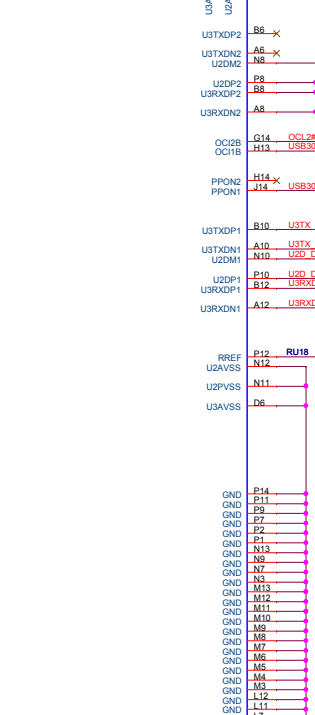
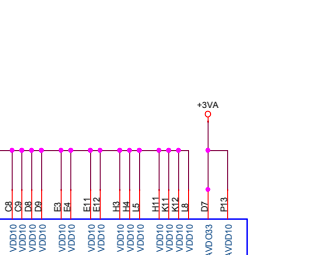
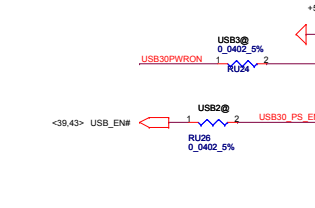
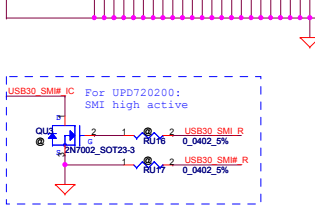
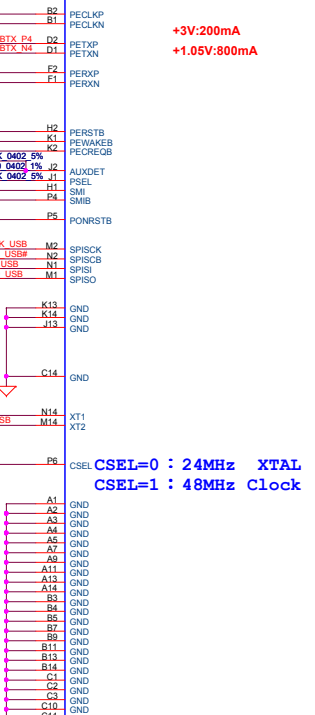
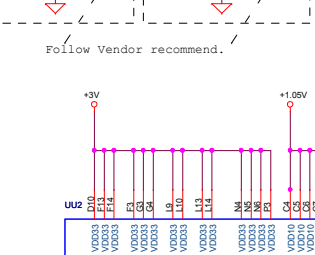
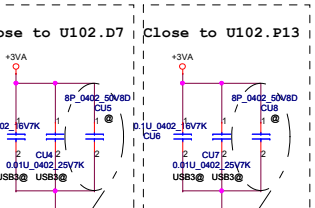
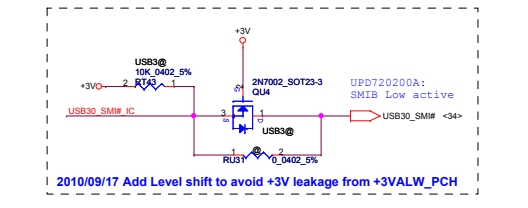
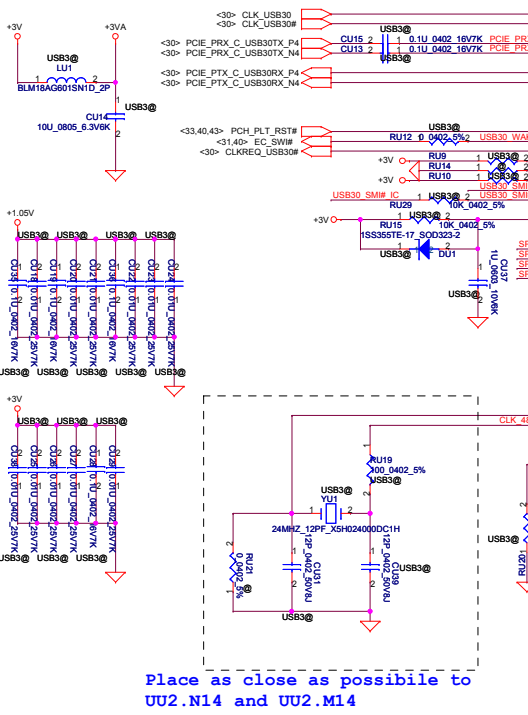
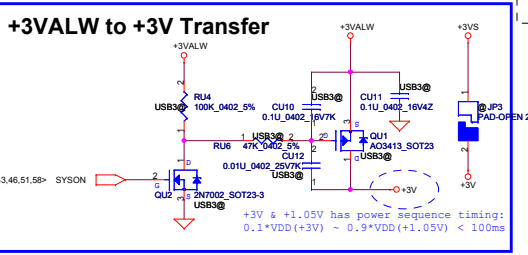
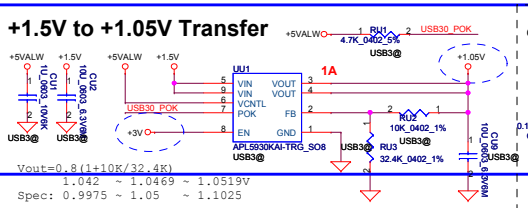
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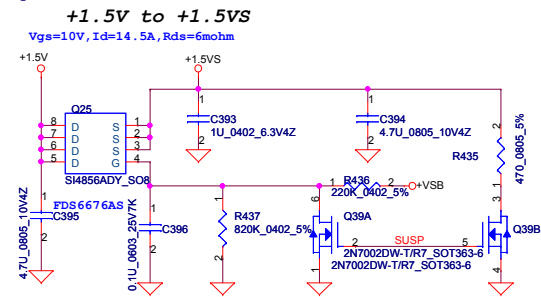
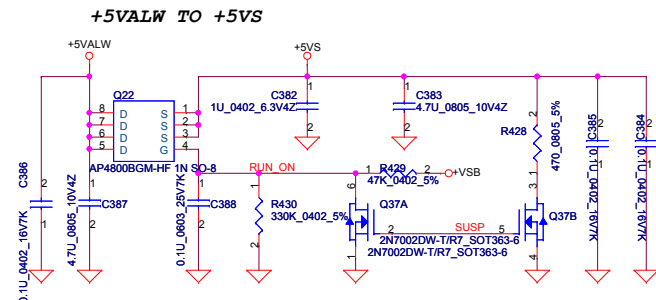
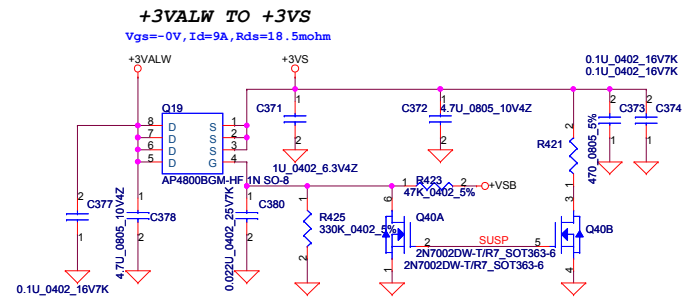
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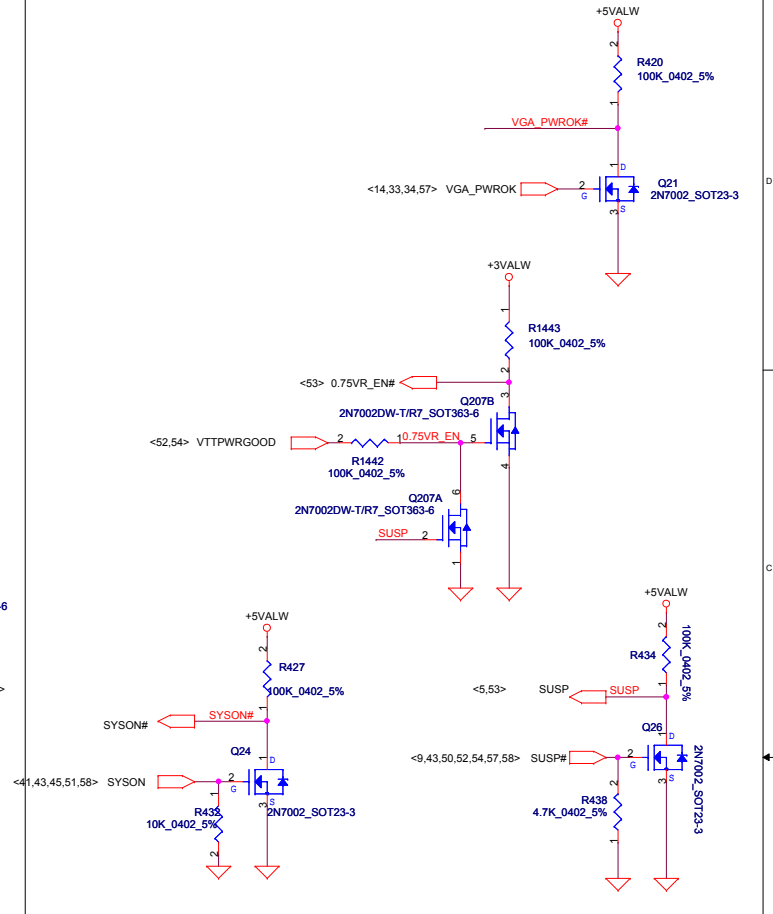
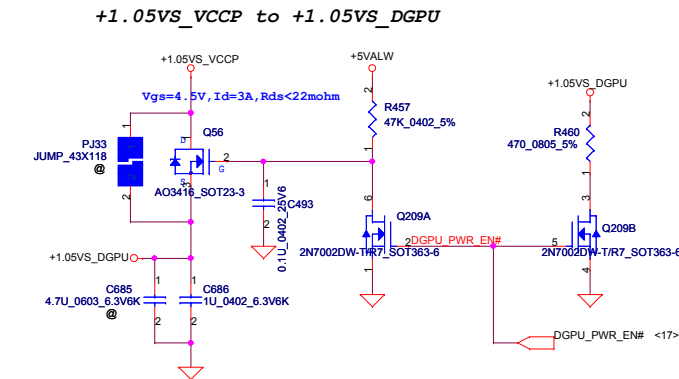
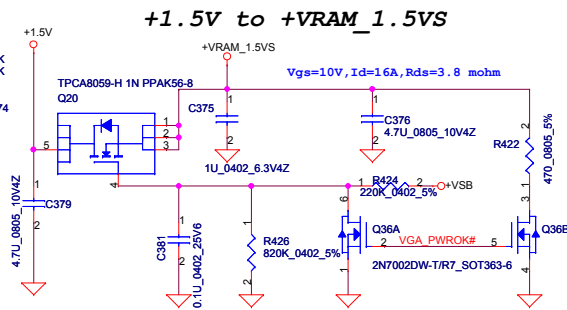
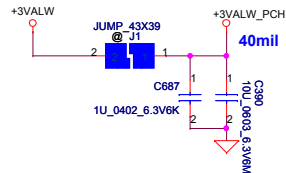
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			Friday, January 21, 2011			Sheet	45	of 58

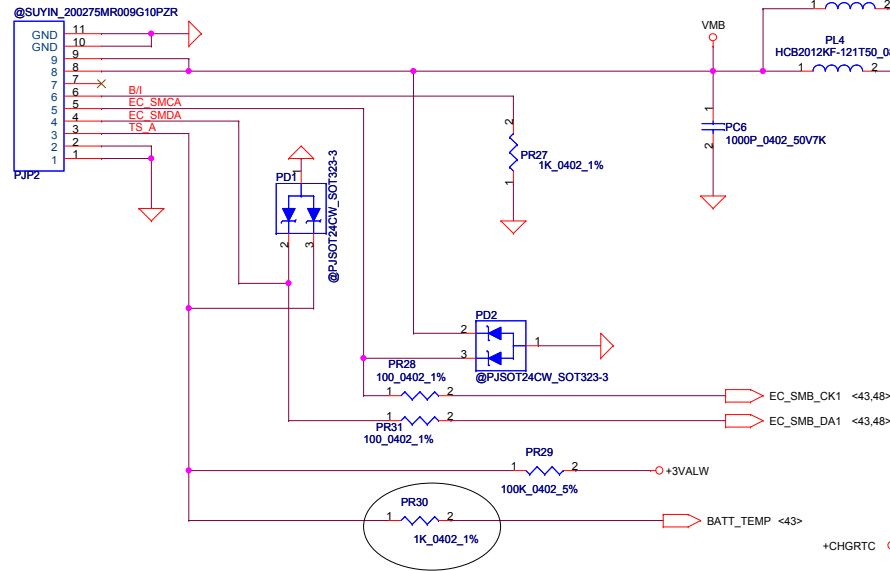
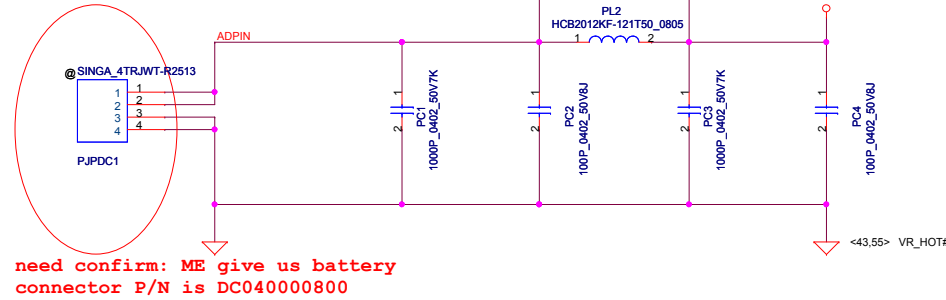


+3VALW TO +3VALW(PCH AUX Power)
Short J1 for PCH VCCSUS3.3

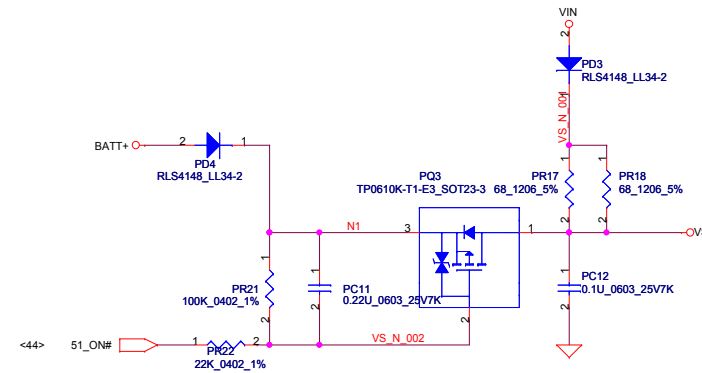
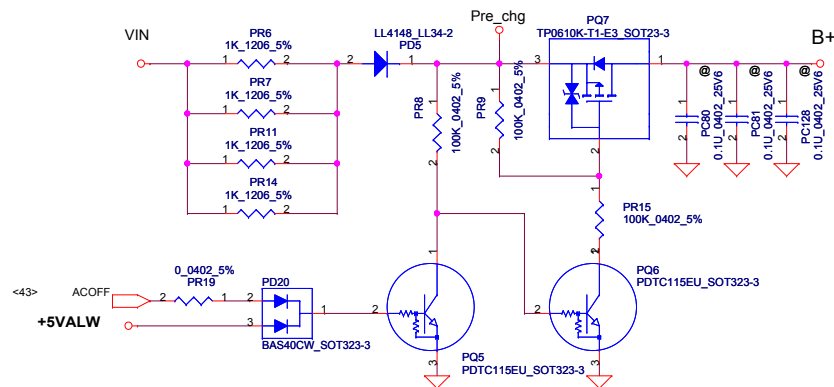
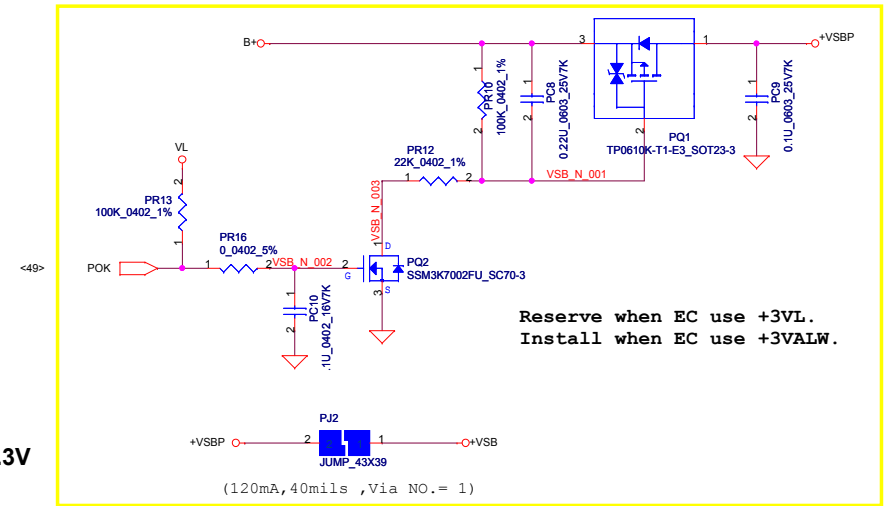
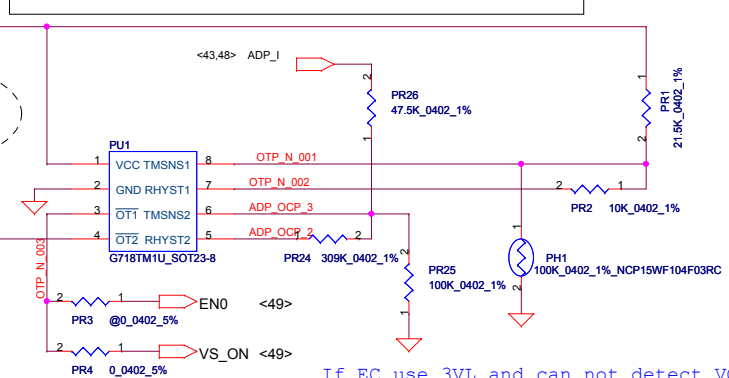


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				2011/12/03				PBL80 LA-7441P M/B			
								Rev 0.1			
								Date: Friday, January 21, 2011			
								Sheet 46 of 58			

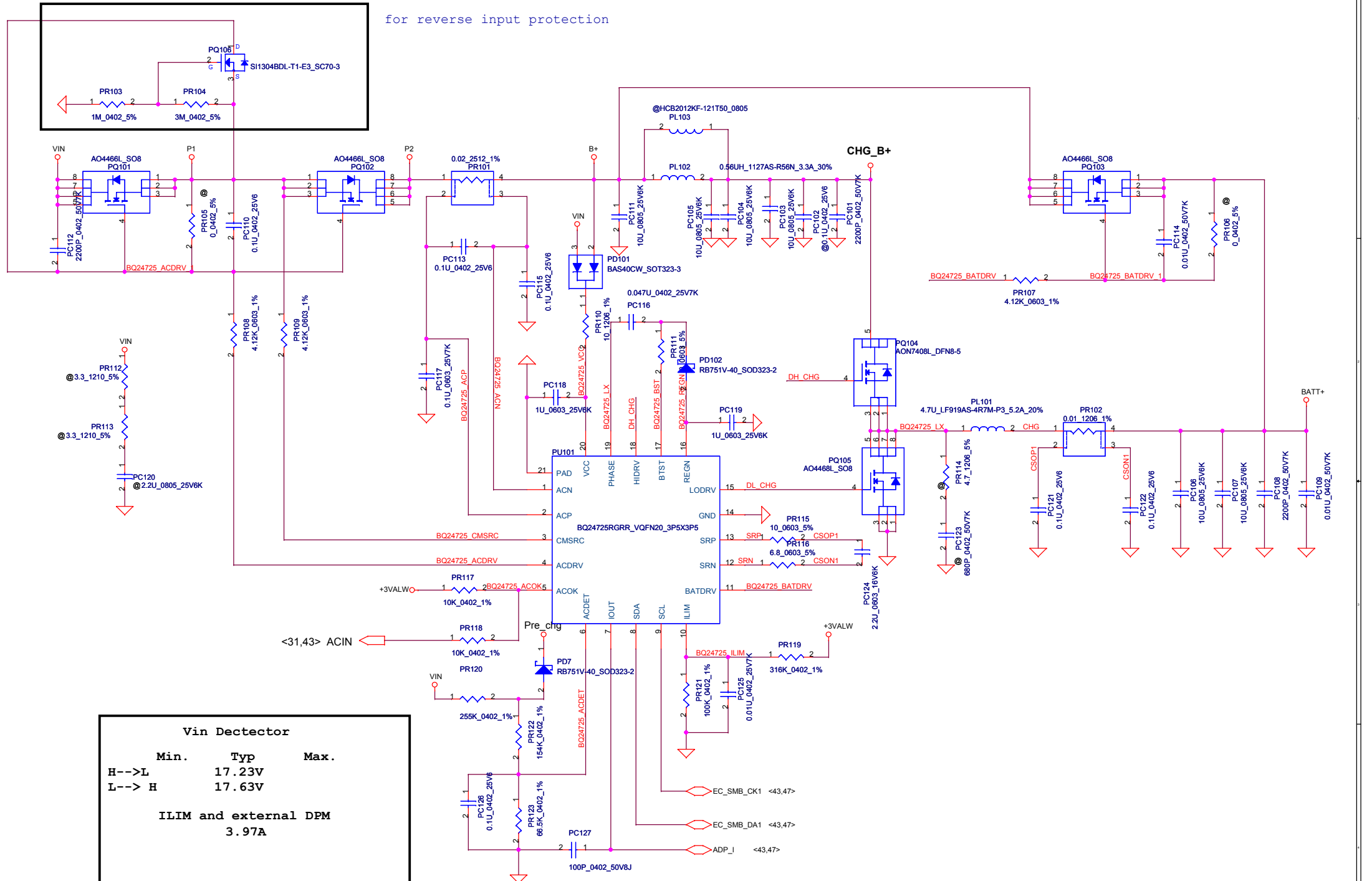
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



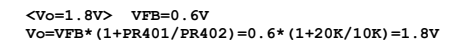
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



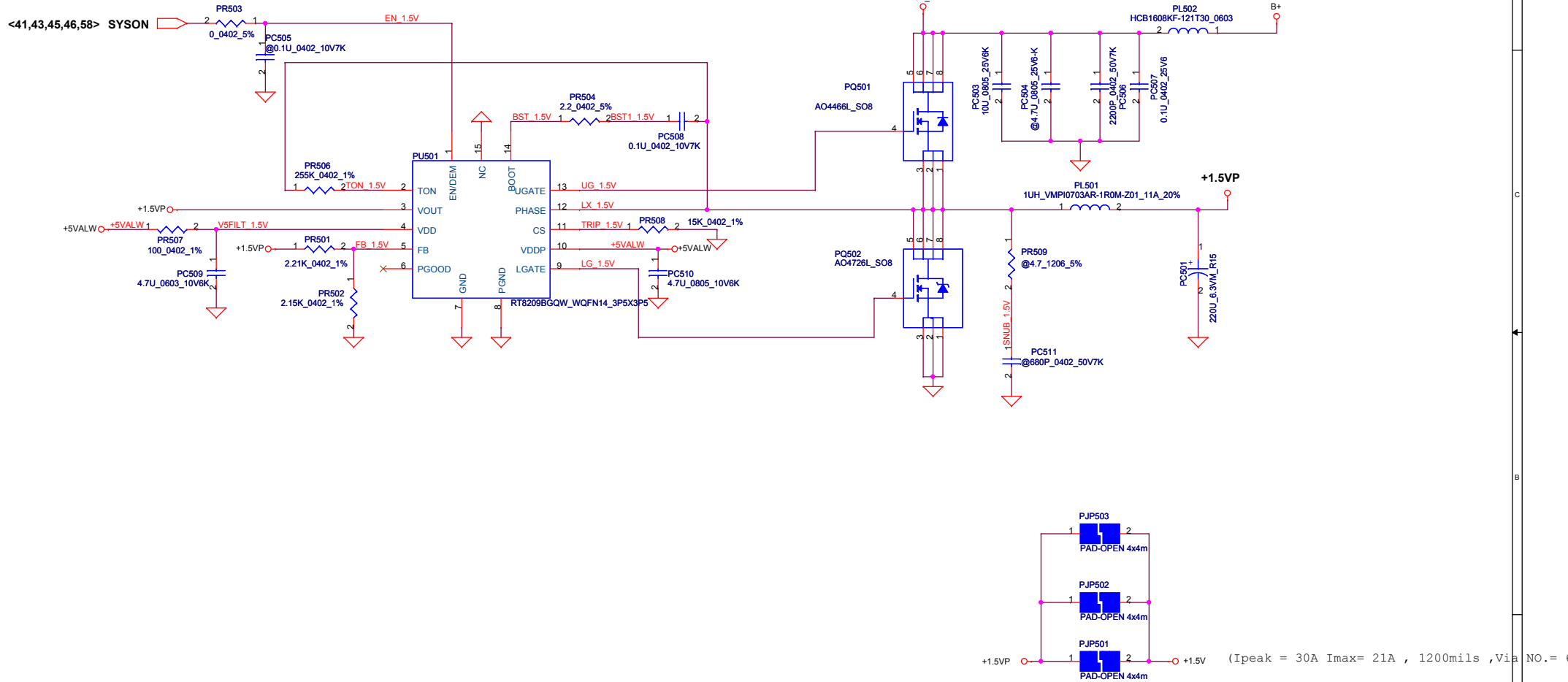
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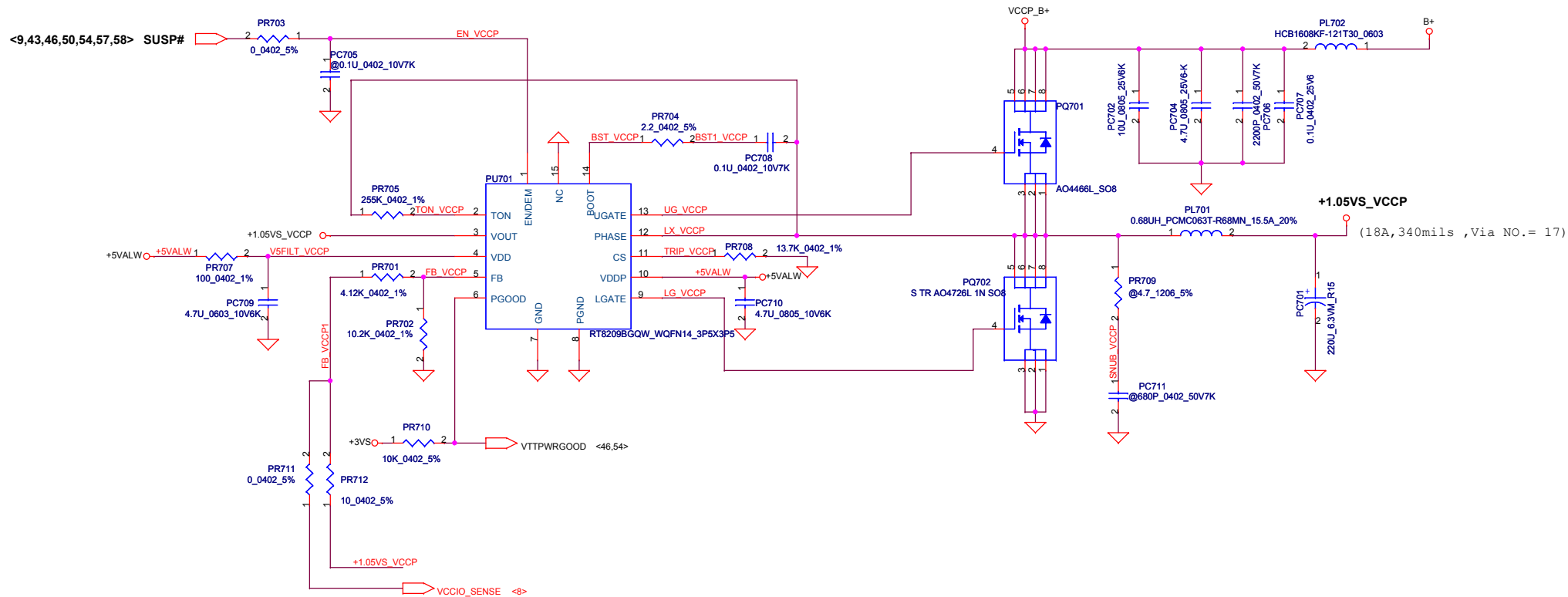
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				Date:	Friday, January 21, 2011
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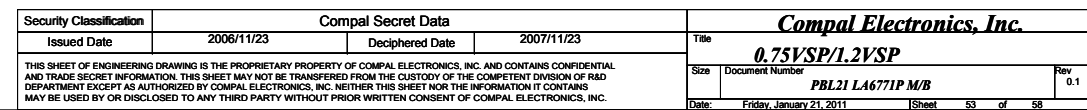
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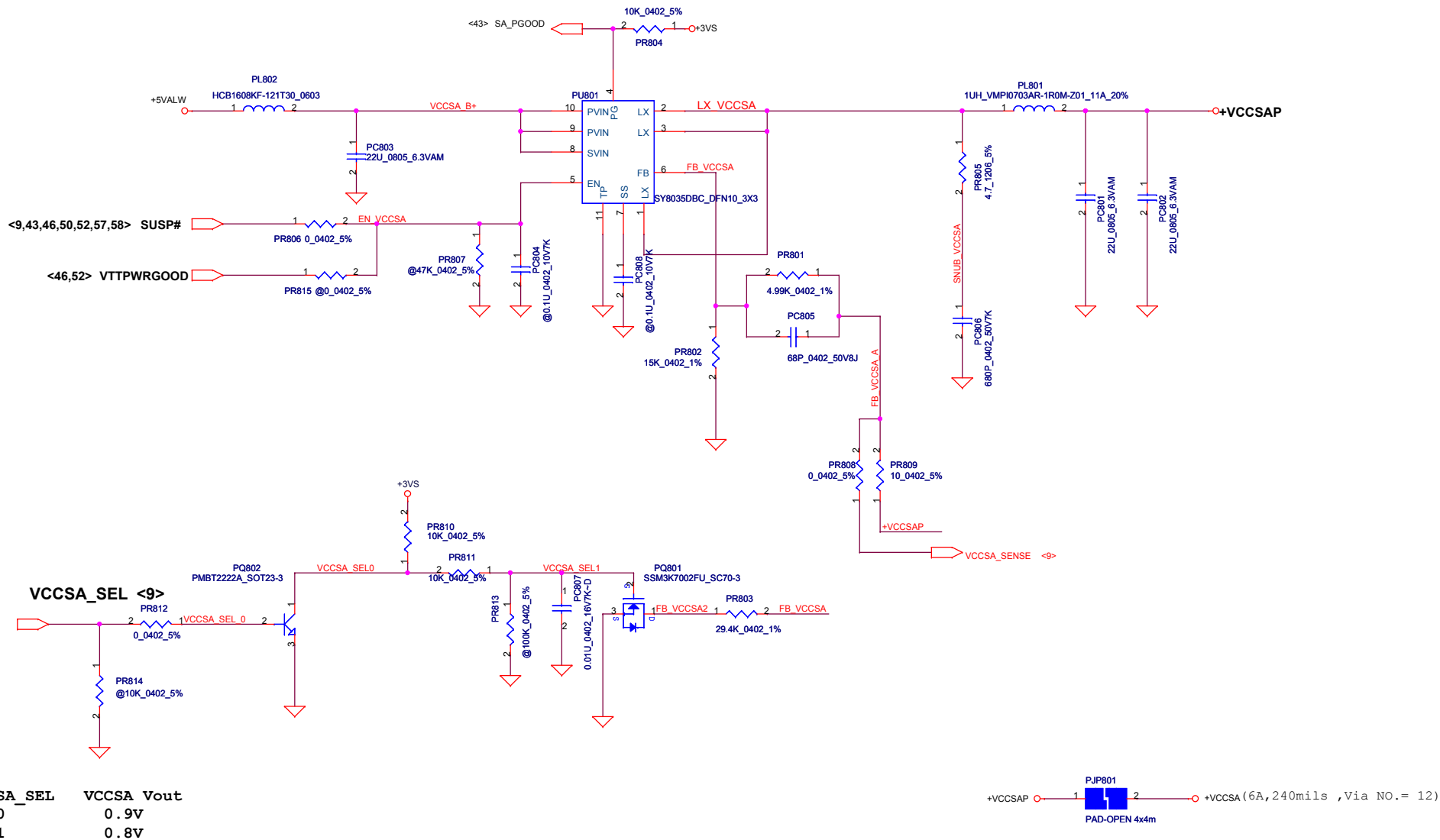


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				Date	Friday, January 21, 2011
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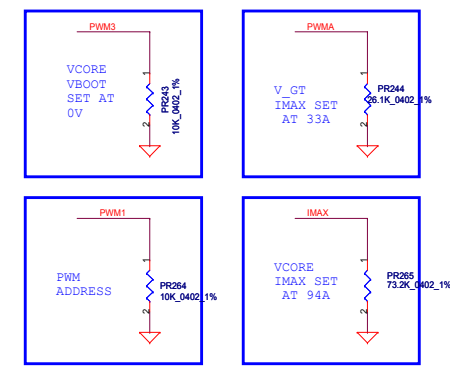
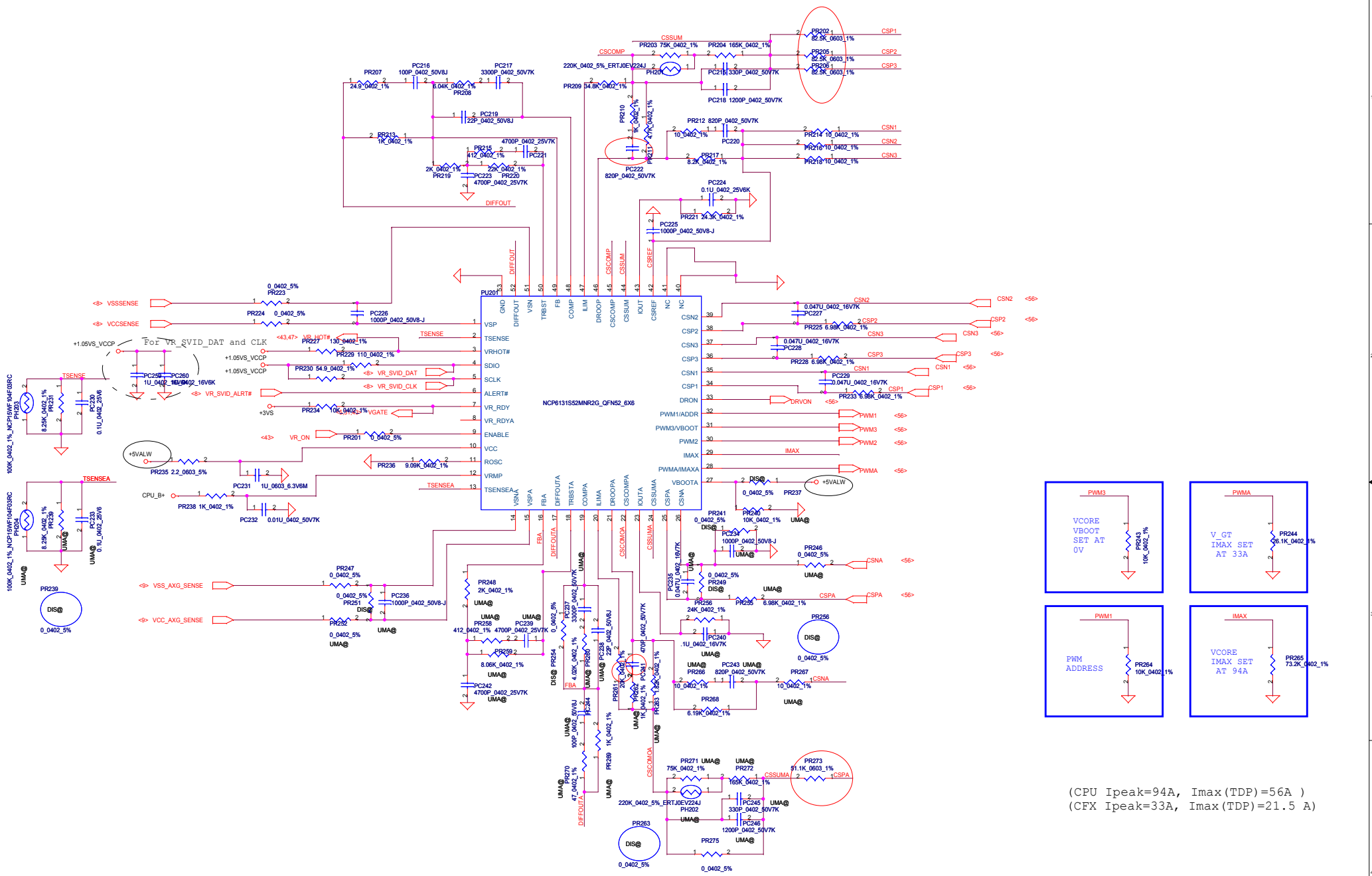


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				Sheet	52 of 58
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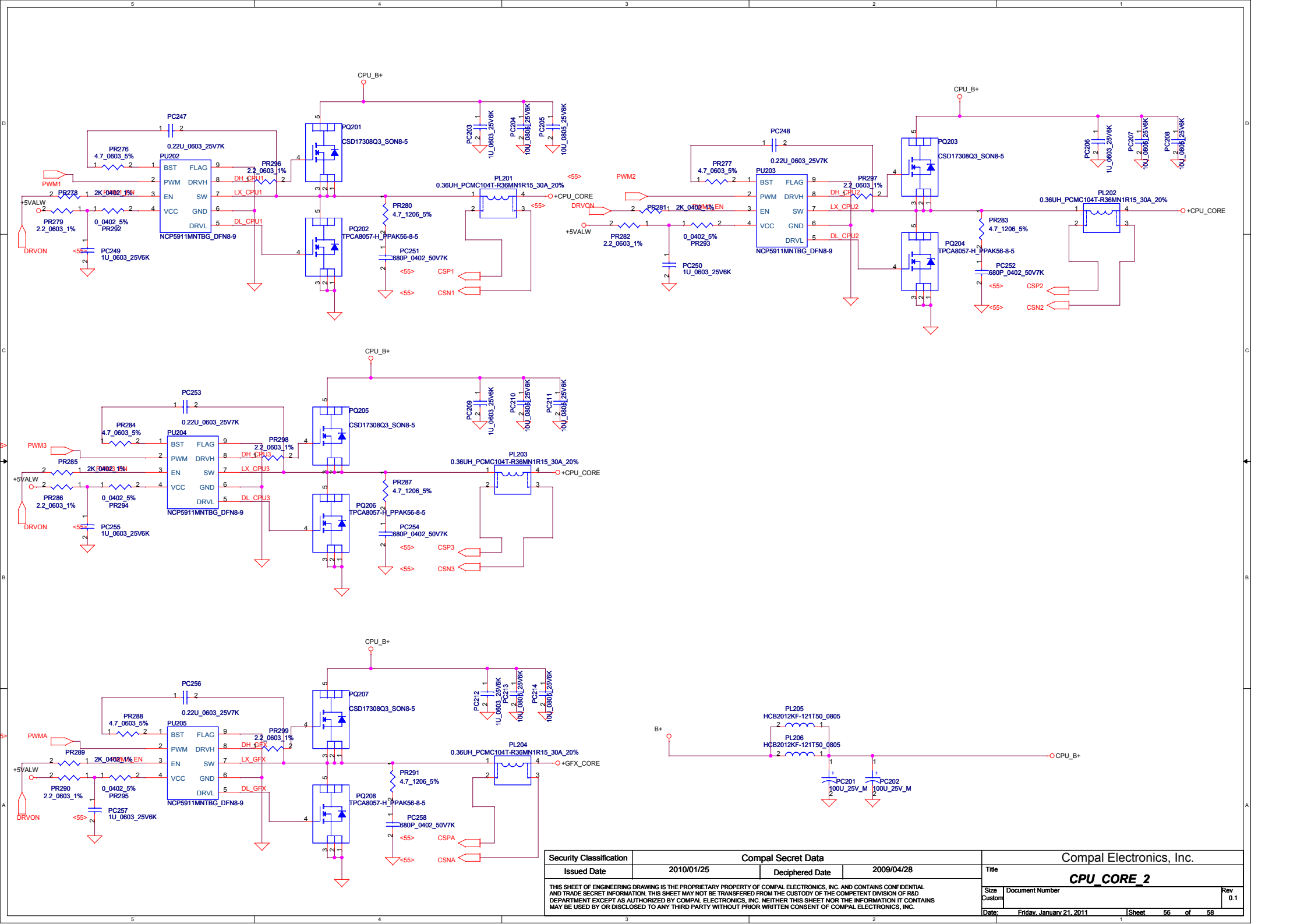


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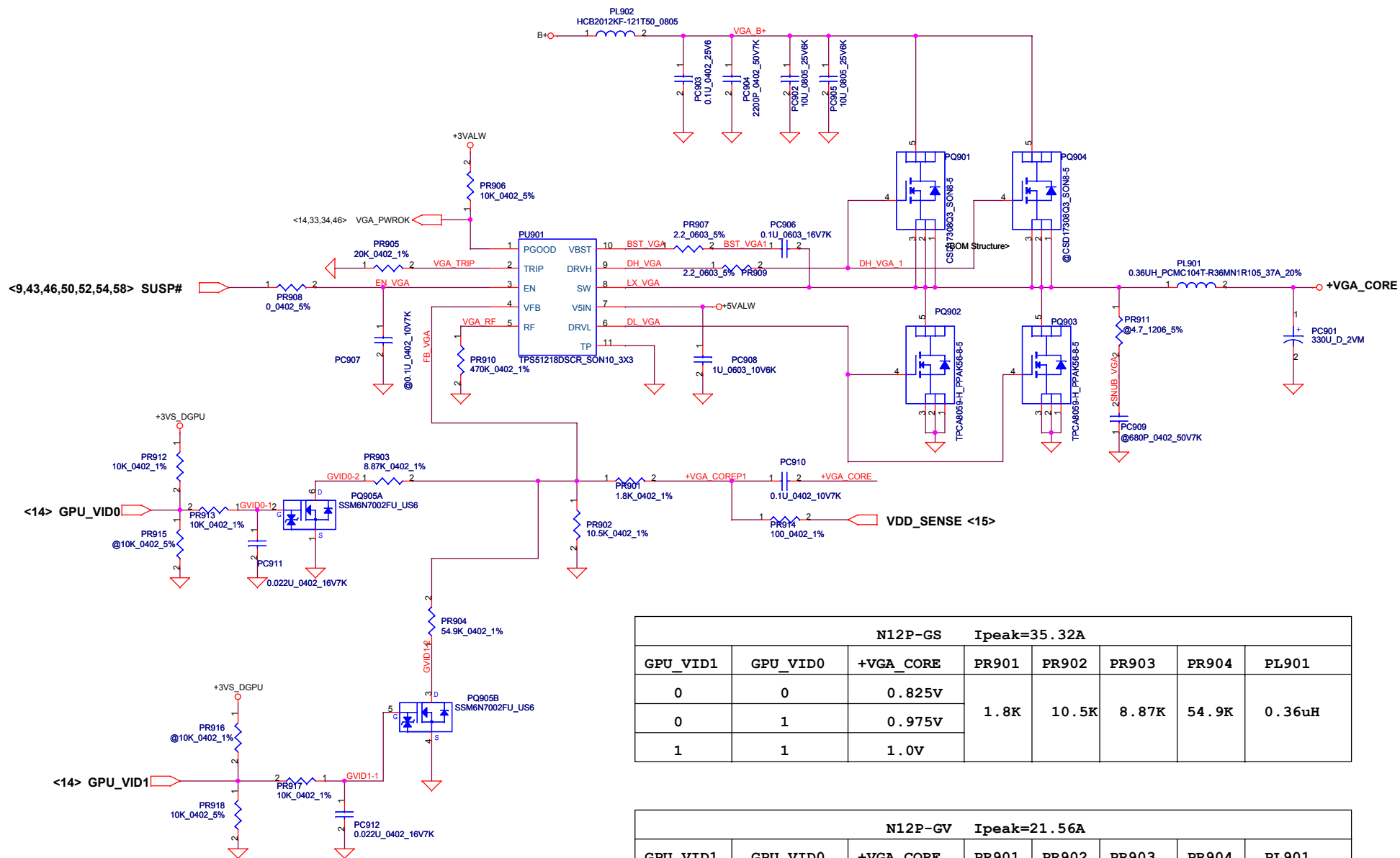


(CPU Ipeak=94A, Imax(TDP)=56A)
(CFX Ipeak=33A, Imax(TDP)=21.5 A)

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2010/01/25		2009/04/28		CPU CORE 1	
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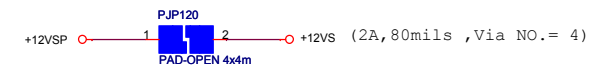
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N12P-GS Ipeak=35.32A						
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904
0	0	0.825V	1.8K	10.5K	8.87K	54.9K
0	1	0.975V				
1	1	1.0V				

N12P-GV Ipeak=21.56A						
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904
0	0	0.85V	1.8K	10.5K	8.87K	54.9K
0	1	1.0V				
1	1	1.025V				

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								Size	Document Number						Rev
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